# High performance storage systems technology update and introduction to 12G physical layer validation

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# Agenda: High performance storage systems technology update and introduction to 12G physical layer validation

- Introduction
  - Industry Timeline
  - SATA 3.1 Spec Revisions
    - UTD 1.4.3 overview
    - SATA/PCIE: SATAExpress Convergence
  - SAS 3.0 r0 Spec Introduction and Measurement Considerations at ~12G
    - 12+ G Design Problem
    - Crosstalk
    - BUJ
    - WDP
    - Signal Amplitude
    - Instrumentation


REFERENCES

(1) Richard Mellitz: Intel: T10/ 11-275r0 SAS-3 12Gbs Transmitter Device Test Proposal

(2) Doron Lapidot: Tyco: T10/10-219r0 SAS 3.0 B-t-B Connector & Cable assembly Channel Performance @ 12Gbps "Modeling, Measurements & Simulations for BER compliance with multi Aggressor System Interconnect"

(3) Mickey Felton: EMC: T10/11-239r0 Channel compliance points and lengths

(4) Kevin Witt: Maxim: T10/11-221r4 SAS-3 Electrical Spec (Draft)

(5) Mathieu Gagnon : PMC-SIERRA: T10/11-008r3 SAS-PHY: SAS3_EYEOPENING update

(6) Mladen Luksic: SATA-IO: IW12 Roadmap Update

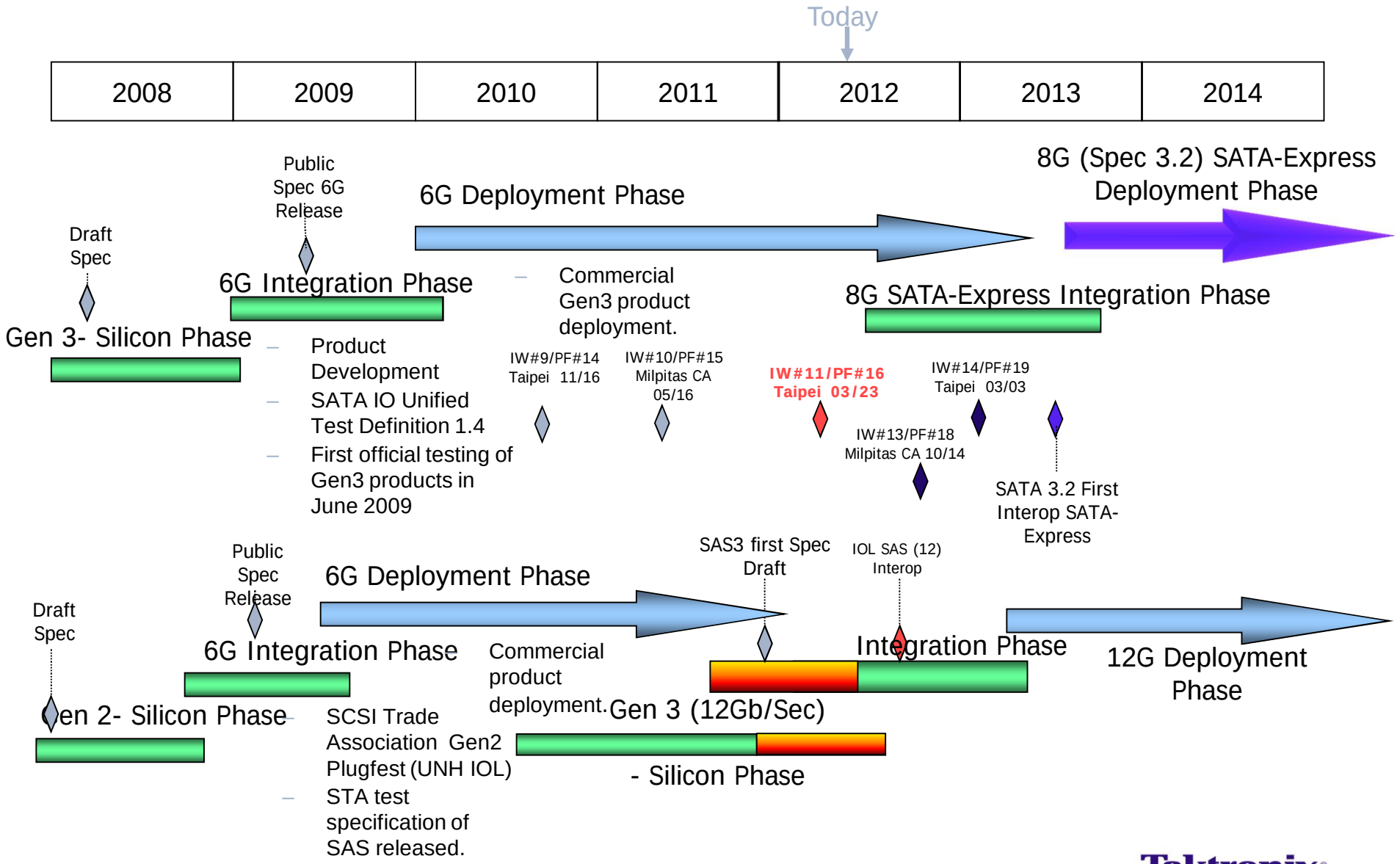
General REFERENCES:

[1] IEEE is 25Gb/s on-board signaling Viable? KAM et al.: IEEE Transactions on advanced Packaging, Vol. 32, No. 2, May 2009.

[2] IEEE CMOS SerDes core with feed-forward and decision-feedback equalization . T. Beukem et al.: IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2633–2645

[3] Alcatel-Lucent: DSP & FEC: Towards the Shannon Limit Timo Pfau ECOC'09 | WS1: DSP & FEC | Sept. 20, 2009

# Storage Timelines and Solutions Development



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# SATA 3.1/ UTD 1.4.3 Spec Revisions

It's the measurements ..

# SATA UTD 1.4.3 Test Requirements

| Phy Transmit Signal Requirements | |
|---|---|
| TSG-01 : Differential Output Voltage | |
| TSG-02 : Rise/Fall Time | revised |
| TSG-03 : Differential Skew | |
| TSG-04 : AC Common Mode Voltage | revised |
| TSG-05 : Rise/Fall Imbalance | |
| TSG-06 : Amplitude Imbalance | obsolete |
| TSG-07 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/10 | |
| TSG-08: Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/10 | |
| TSG-09 : Gen1 (1.5Gb/s) TJ at Connector, Clock to Data, fBAUD/500 | |
| TSG-10 : Gen1 (1.5Gb/s) DJ at Connector, Clock to Data, fBAUD/500 | |
| TSG-11 : Gen2 (3Gb/s) TJ at Connector, Clock to Data, fBAUD/500 | |
| TSG-12 : Gen2 (3Gb/s) DJ at Connector, Clock to Data, fBAUD/500 | |
| TSG-13: Gen3 (6Gb/s) Transmit Jitter w/wo CIC | revised |
| TSG-14 : Gen3 (6Gb/s)TX Maximum Differential Voltage Amplitude | |
| TSG-15 : Gen3 (6Gb/s) TX Minimum Differential Voltage Amplitude | ECN-50 Revised |
| TSG-16 : Gen3 (6Gb/s) Tx AC Common Mode Voltage | revised |

| Phy Receive Signal Requirement | |
|---|---|
| RSG-01 : Gen1 (1.5Gb/s) Receiver Jitter Tolerance Test (Normative) | |
| RSG-02 : Gen2 (3Gb/s) Receiver Jitter Tolerance Test (Normative) | |
| RSG-03 : Gen3 (6Gb/s) Receiver Jitter Tolerance Test | ECN-50/ECN-51 Revised |
| RSG-05 : Gen1 Asynchronous Receiver Stress Test at +350ppm | |
| RSG-06 : Gen1 Asynchronous Receiver Stress Test With SSC | |

| SI General Requirements |
|---|
| SI-1:8 : Cable Characterization |
| SI-09 : Inter-Symbol Interference |

| Phy General Requirements |
|---|
| PHY-01 : Unit Interval |
| PHY-02 : Frequency Long Term Stability |
| PHY-03 : Spread-Spectrum Modulation Frequency |
| PHY-04 : Spread-Spectrum Modulation Deviation |

| Phy OOB Requirements |
|---|
| OOB-01 : OOB Signal Detection Threshold |
| OOB-02 : UI During OOB Signaling |
| OOB-03 : COMINIT/RESET and COMWAKE Transmit Burst Length |
| OOB-04 : COMINIT/RESET Transmit Gap Length |
| OOB-05 : COMWAKE Transmit Gap Length |

| Phy Receiver/Transmitter Channel Reqs | |
|---|---|
| RX/TX-01 : Pair Differential Impedance | |
| RX/TX-02 : Single-Ended Impedance (Obsolete) | |
| RX/TX-03 : Gen2 (3Gb/s) Differential Mode Return Loss | informative |
| RX/TX-04 : Gen2 (3Gb/s) Common Mode Return Loss | |
| RX/TX-05 : Gen2 (3Gb/s) Impedance Balance | |
| RX/TX-06 : Gen1 (1.5Gb/s) Differential Mode Return Loss | |
| RX/TX-07 : Gen3 (6Gb/s) Differential Mode Return Loss | |
| RX/TX-08 : Gen3 (6Gb/s) Impedance Balance | |

**SATA Measurement Legends:**

- No change from previous UTD 1.3 spec version
- Revised methodology from UTD1.3 to UTD 1.4
- New test definitions in UTD 1.4
- Obsolete

Summary: TSG05/06 have been classified as EMI related and moved to an obsolete status. TSG15 will use an eye height methodology and will have different limits depending on the DUT being a Host or Device



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# SATA ECN 50: Asymmetric Amplitude and Measurement Methodology

- Host and Device Transmitter signal amplitude asymmetry has now been instituted in the SATA 3.1 specification.

| Parameters | Units | Limit | Electrical Specification | | | | | Detail Cross-Ref Section | Measurement Cross-Ref Section |
|---|---|---|---|---|---|---|---|---|---|
| | | | Gen1i | Gen1m | Gen2i | Gen2m | Gen3i | | |
| $SSC_{tol}$, Spread-Spectrum Modulation Rate | ppm/ usec | Max | 1250 | | 1250 | 1250~~-~~ | | 7.2.2.1.6 7.3.3 | 7.4.15 |

| Parameter | Units | Limit | Electrical Specification | | | | | Detail Cross-Ref Section | Measurement Cross-Ref Section |
|---|---|---|---|---|---|---|---|---|---|
| | | | Gen1i | Gen1m | Gen2i | Gen2m | Gen3i | | |
| $V_{diffTXdevice}$, TX Differential Device Output Voltage | mVppd | Min | 400 | | 400 | | - | 7.2.2.3 | 7.4.6 |
| | | Min | - | | - | | 240 | | 7.4.4 7.4.4.3 |
| | | Nom | 500 | | - | | - | | 7.4.6 |
| | | Max | 600 | | 700 | | - | | |
| | | Max | - | | - | | 900 | | 7.4.4 |
| $V_{diffTXhost}$, TX Differential Host Output Voltage | mVppd | Min | 400 | | 400 | | - | 7.2.2.3 | 7.4.6 |
| | | | - | | - | | 200~~240~~ | | 7.4.4 7.4.4.3 |
| | | Nom | 500 | | - | | - | | 7.4.6 |
| | | Max | 600 | | 700 | | - | | |
| | | Max | - | | - | | 900 | | 7.4.4 |
| $UI_{VminTX}$, TX Minimum Voltage Measurement Interval | UI | | 0.45-0.55 | | 0.45-0.55 | | - | 7.2.2.3.2 | 7.4.6 |
| | | | - | | - | | ~~0.50~~ 0.45-0.55 | | 7.4.6.2 |

- Hosts may signal as low as 200mV (40mV lower than previously allowed)
- Devices must retain the original 240mV levels.
- Measurement methodology has been revised from a vertical BER contour to a simple Eye Height measurement.



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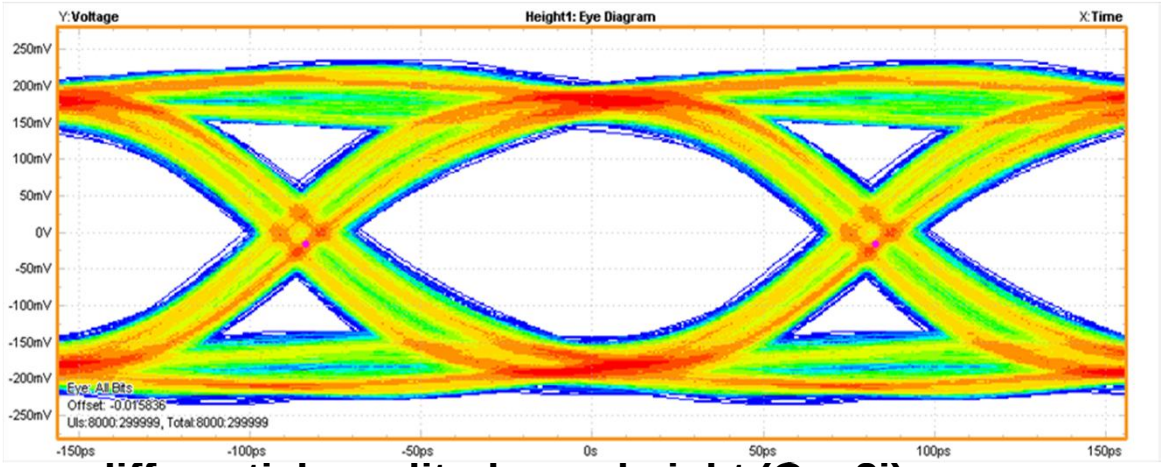
# SATA ECN 50: Asymmetric Amplitude and Measurement Methodology (cont)

- Due to the changes to the minimum Tx levels receiver test protocols have now been revised to calibrate for Host and Device amplitudes differently.




**7.4.3.3 Minimum differential amplitude eye height (Gen3i)**

4 Sigma Eye Diagram constructed from a minimum 5E6 number of unit intervals with either mean based PLL or an explicit clock or mean based clock equivalent.

**Receiver Test Calibration levels and method details.**

200mV for Drive side receiver (Eye Height + CIC + Explicit Clock)

240mV for the Host side receiver (Eye Height + CIC + Explicit Clock)

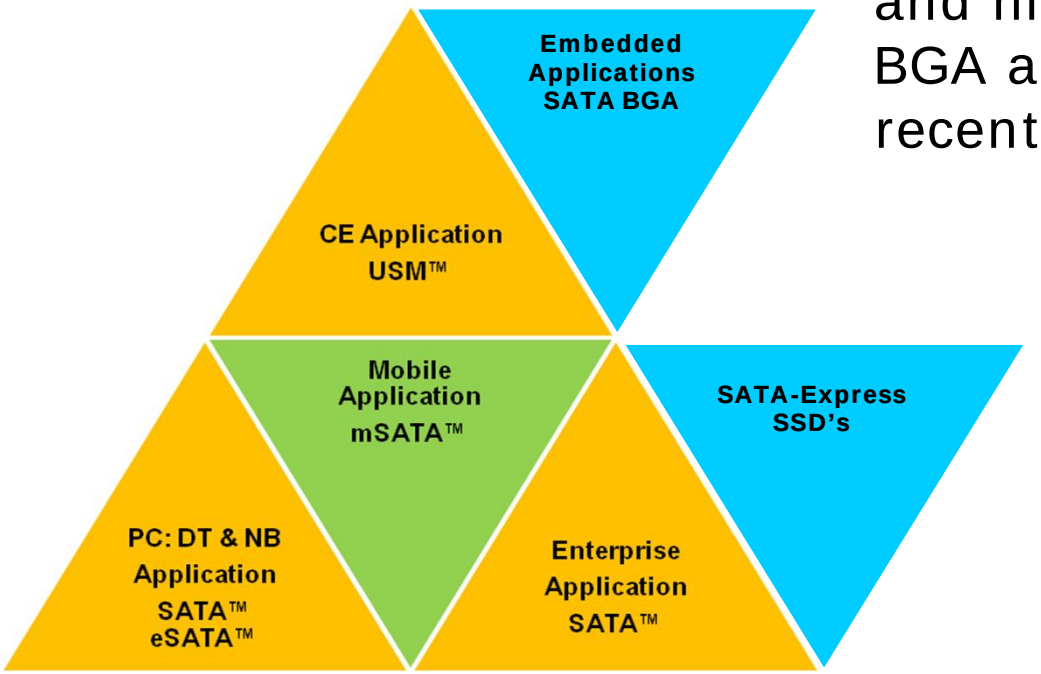
**Transmitter Test levels and method details.**

240mV for Drive side transmitter minimum (Eye Height + CIC + JTF PLL)

200mV for the Host side transmitter minimum (Eye Height + CIC + JTF PLL)

The Eye Height is to be evaluated at the 50% UI location.

# The SATA Ecosystem: Now




Today, SATA is expanding in specialized low power, compact and high performance areas with BGA and SATA-Express Solutions recently approved by SATA-IO.



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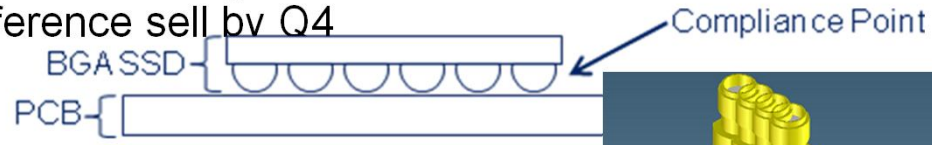
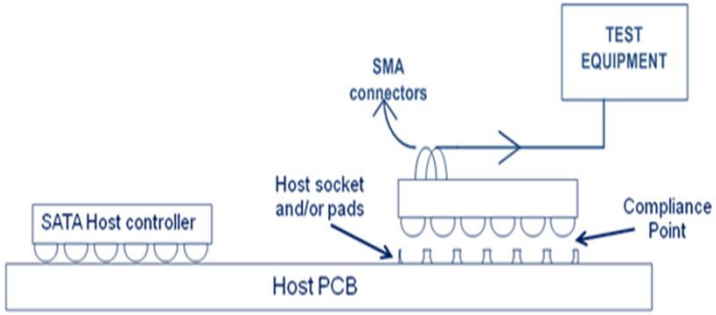
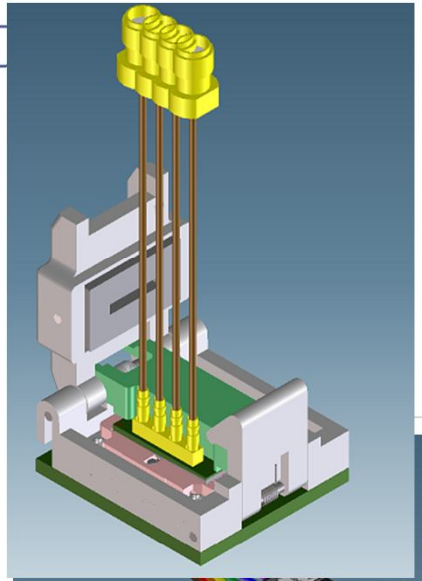
# New SSD's approved by SATA-IO

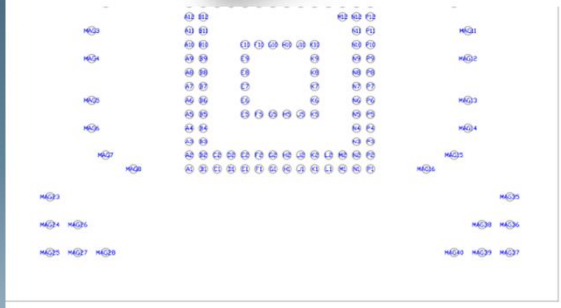
- Test Strategy: Two BGA based fixtures are being commissioned with Wilder through SATA-IO. Target available through reference sell by Q4

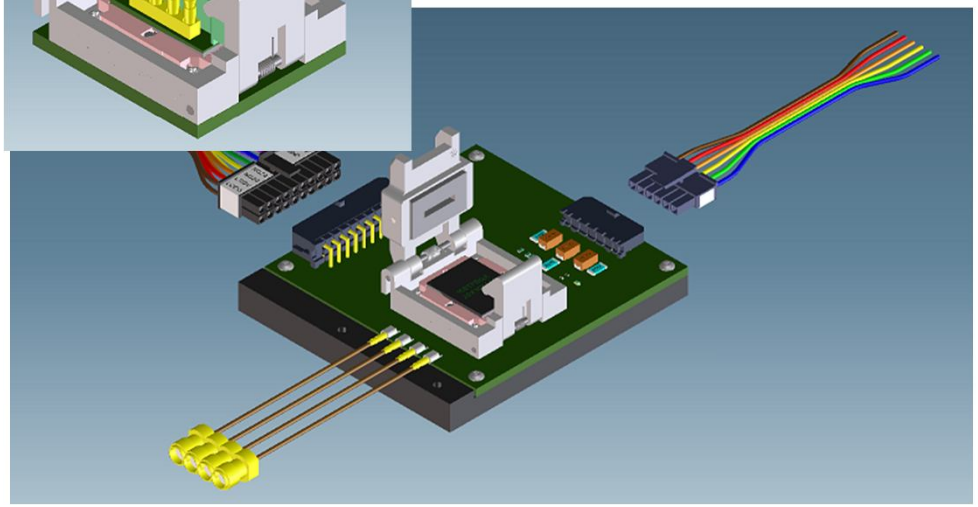


- Host Fixture: A BGA breakout to SMA's which will be re-flowed onto the motherboard.







- Device Fixture: A carrier with a uBGA Socket Connector onto the motherboard.



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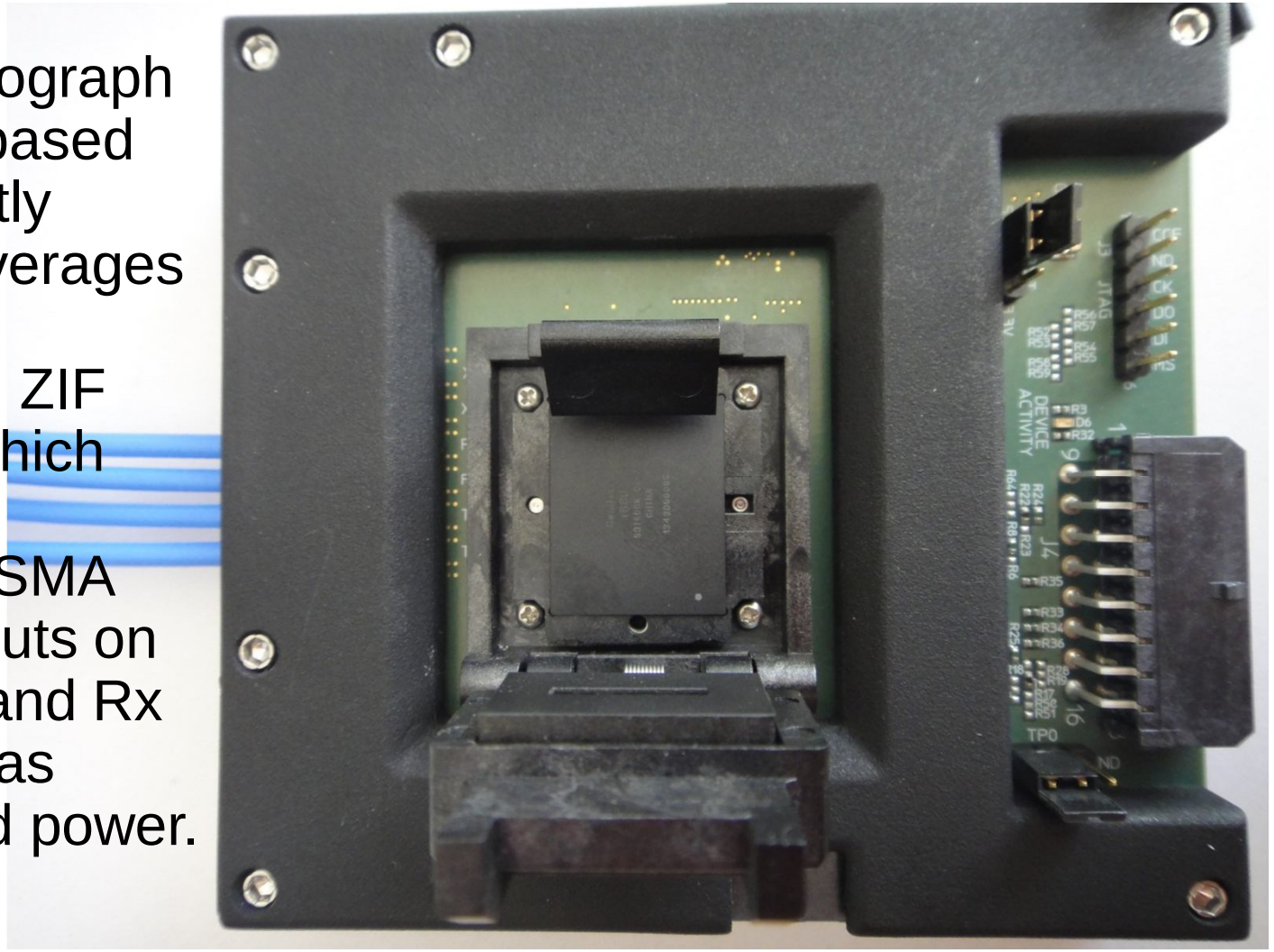
# *u*BGA based test configuration. Wilder fixture shown.

- This is a photograph of the uBGA based system recently tested . It leverages the Wilder Technologies ZIF BGA fixture which presents conventional SMA based breakouts on the SATA Tx and Rx lines, as well as DevSleep and power.



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# PCIe

- PCIe is multi-lane → scalable
  - 1 to 16 lanes
- PCIe (Gen3) each lane is 8 Gbps → 1 GB/sec
  - no 8b/10b encoding
- It is already available
- PCIe is **NOT** a replacement for SATA

PCIe is the obvious choice



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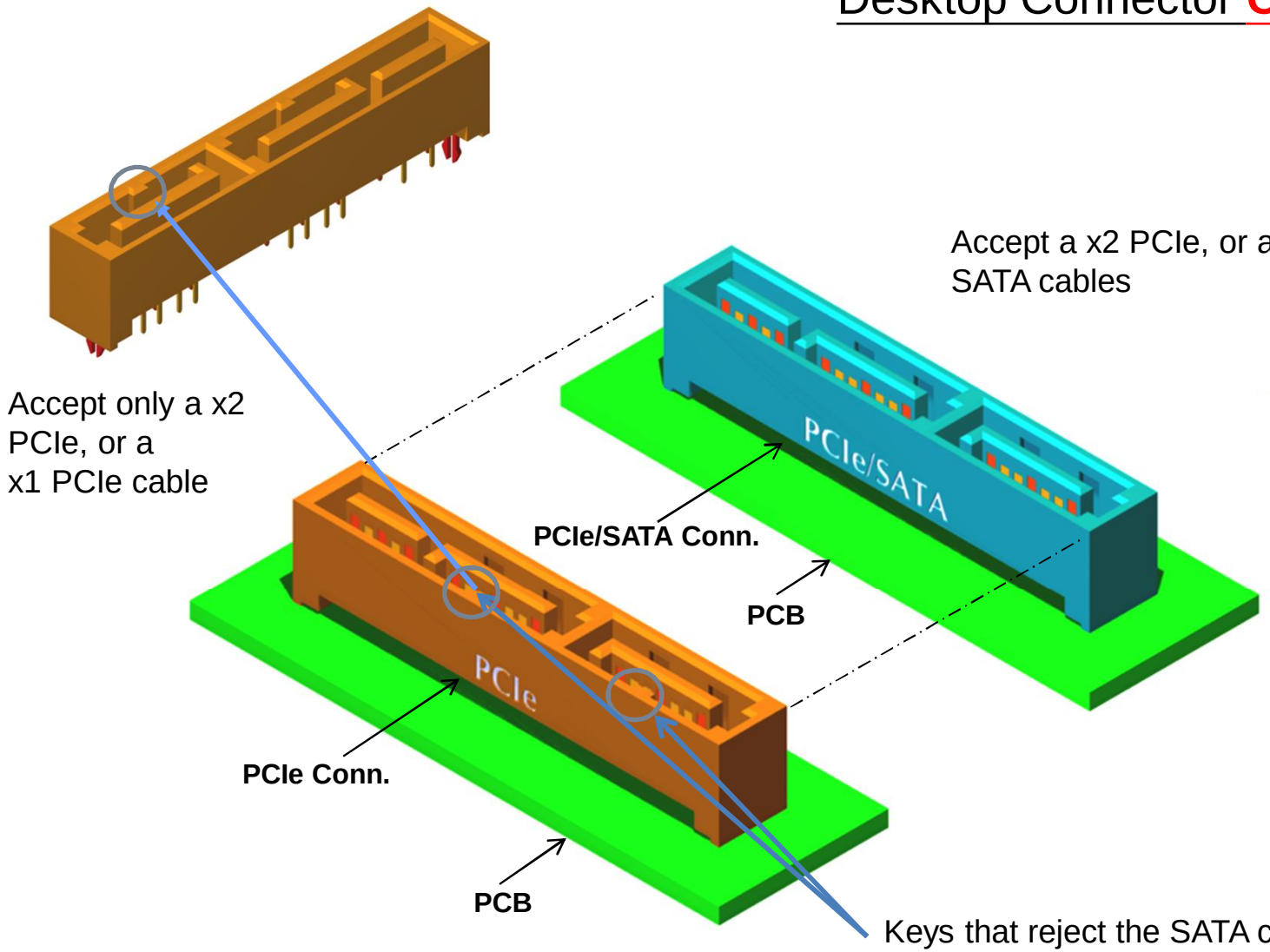
# Enabling the New SATA Express Ecosystem

Desktop Connector **Concept**


Accept only a x2 PCIe, or a x1 PCIe cable
Accept a x2 PCIe, or a x1 PCIe, or two SATA cables
PCIe/SATA
PCIe/SATA Conn.
PCB
PCIe
PCIe Conn.
PCB
Keys that reject the SATA cables



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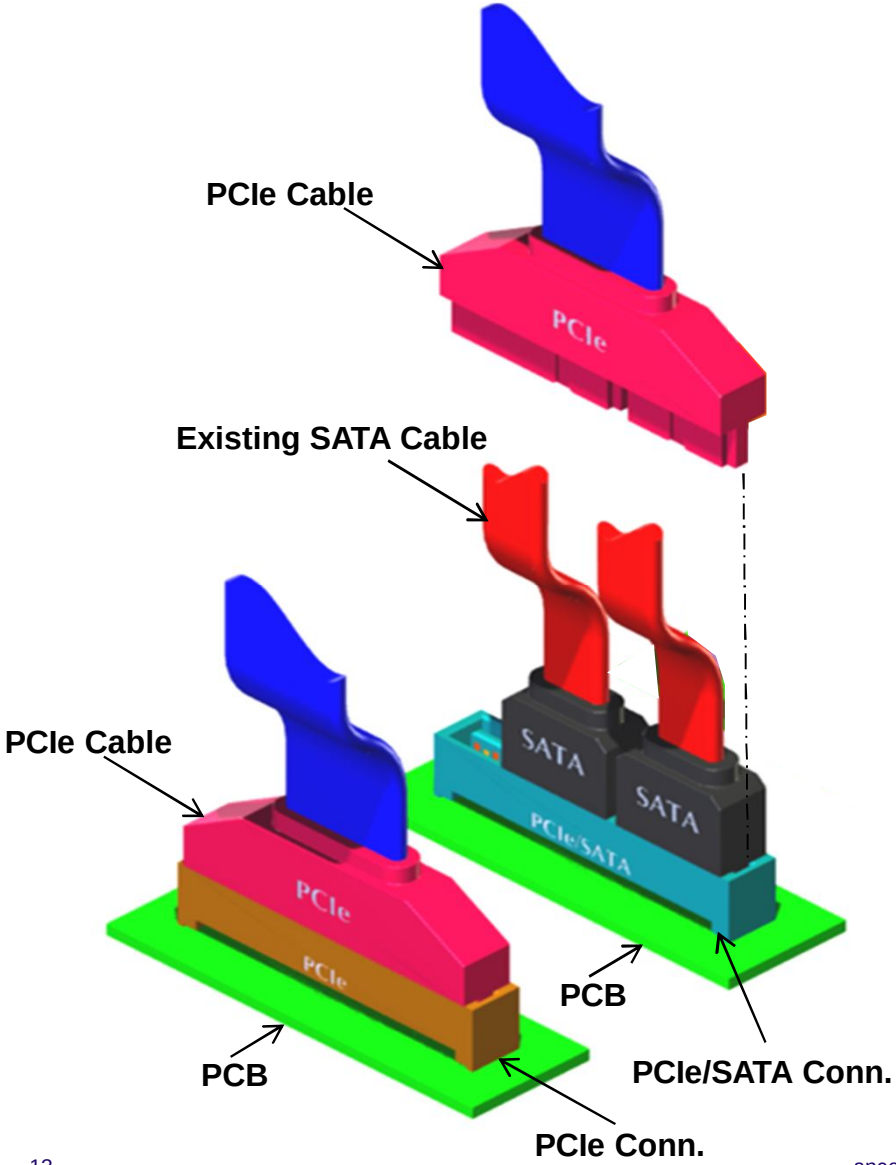
# Enabling the New SATA Express Ecosystem




## Desktop Cables **Concept**

SATA devices will coexist with next generation PCIe devices

SATA cost/performance benefits

Requires a connector that supports both PCIe and SATA

- Allows a single motherboard (backplane) connector to support both interfaces

HDD-compatible form factors to be defined for PCIe devices

- Enables system-level mechanical compatibility
- Preserves high-capacity storage

SATA-IO CabCon has been chartered to develop SATA compatible connectors and form factors for PCIe SSD/hybrid drives



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# Fundamentals of 12G SAS characterization

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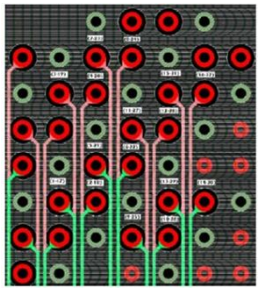
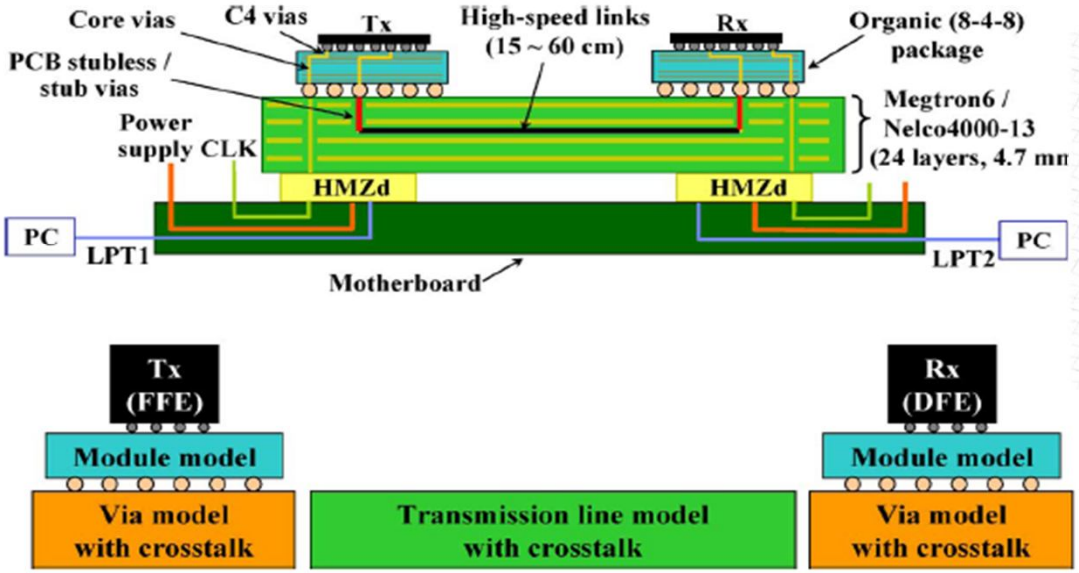
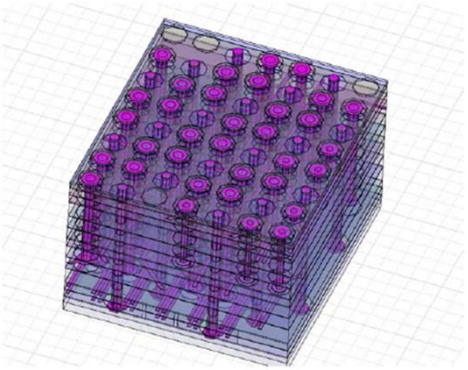
# 12+G Design Problem:
# 1000mV, FFE, Crosstalk, Crosstalk, Crosstalk, DFE, 50mV

- Significant advances in high tap count Decision Feedback Equalization are key to operating at 12+G.
- Mitigating the complex Channel Crosstalk and Signal loss problems which 12+G designs present, is the largest design challenge today.
- Typical Escape Structure bandwidth is 18GHz.
- Crosstalk is often beyond the capability of current equalization architectures to combat, and needs to be quantified if accurate performance projections are to be made based on experimental measurements. For short channels, NEXT may be less of an issue since the insertion loss is not as severe; however, in longer links and at higher data rates it has the potential to become a dominant design consideration. Ref:[1]

KAM *et al.*: IS 25 Gb/s ON-BOARD SIGNALING VIABLE? 329







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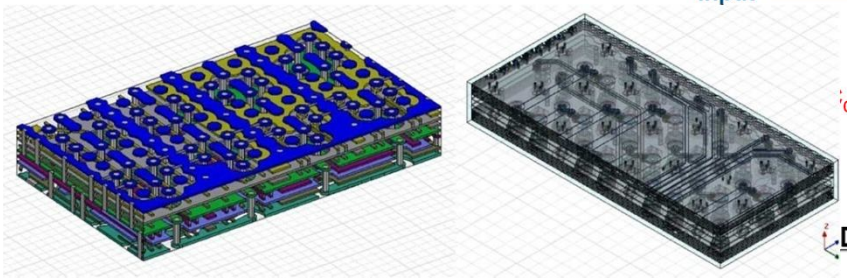
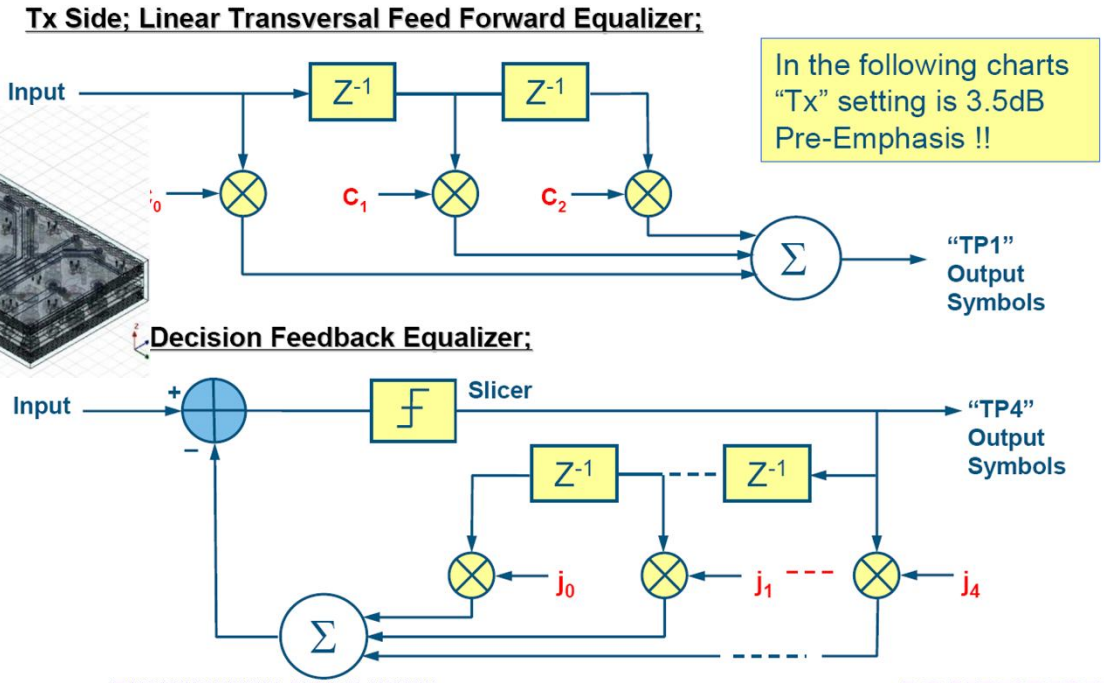
# 12G Design Problem: FFE, DFE

- A non-recursive DFE can only compensate a fixed time span of ISI. In very low-bandwidth channels, significant post-cursor ISI may fall outside the time span covered by the DFE taps.
- FFE can compensate ISI over a very wide time span since the FFE filter response is convolved with the impulse response of the channel.
- The utility of FFE alone drops off rapidly over complex channels which have spectral nulls (Via stubs, connectors, etc) which require many FFE taps to cancel reflections.
- Optimal solutions exist around 4-tap FFE with 20+ (20*60mW) tap DFE designs. More emphasis is required in the Receiver section of the topology as more aggressive FFE makes crosstalk worse.

Ref:[1], [2]

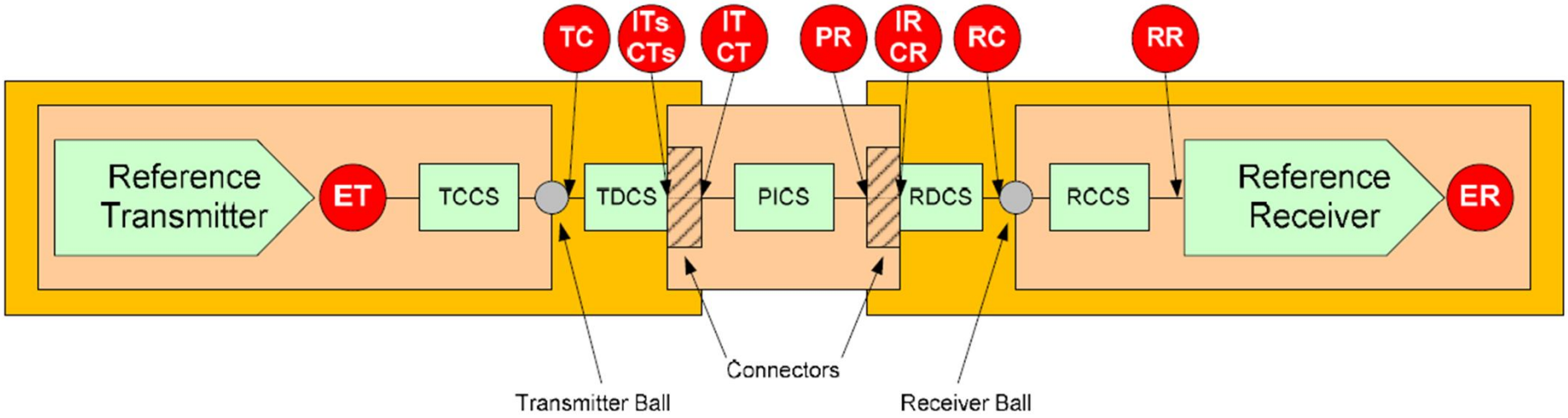




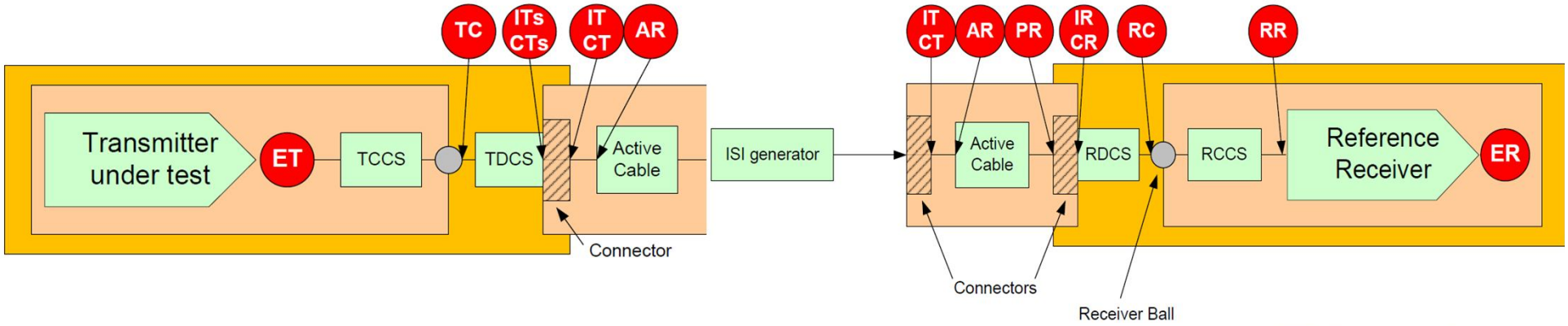

Ref:[2]: Tyco Electronics

# Link Analysis in the context of SAS-12G

- **SAS 12 (Passive Link) Tx Rx Compliance Points.** **(Source 11-416r3)**




- **SAS 12 (Active Link) Active Driver and Receiver Compliance Points**



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# Compliance Points Descriptions

- A TxRx connection is the complete simplex signal path between the transmitter circuit and the receiver circuit
- IT and CT are the only physical measurement points in this system. All other points are modeled or simulated.

| Compliance Point | Compliance Usage | Description |
|---|---|---|
| ET | Transmitter Passive TxRx connection end-to-end simulations | Electrical compliance point for the transmitter, defined at the output of a best-fit reference transmitter for transmitter compliance, or at the output of the reference transmitter for end-to-end simulation. |
| TC | Transmitter | Transmitter circuit compliance point, defined at the transmitter ball. |
| ITs/CTs | Passive TxRx Connection | Silicon side of the transmitter interconnect. |
| IT/CT | Transmitter EqualizationTransmitter end-to-end simulations (ISI characterization) | TxRx connection side of the transmitter interconnect. |
| PR | Receiver assembly stress pattern | TxRx connection side of the receiver interconnect. |
| IR/CR | Passive TxRx Connection | Silicon side of the receiver interconnect. |
| RC | Receiver PHY stress pattern | Receiver circuit compliance point, defined at the receiver ball. |
| RR | Receiver Transmitter maximal output amplitude | Reference receiver input during end-to-end simulations |
| ER | All receiver stress patterns except into active cable receiver<br>All end-to-end simulations except into active cable receiver | Electrical compliance point for the receiver, defined after the reference receiver equalizer. Includes DFE and reference clock recovery. |
| AR | Active cable receiver stress pattern<br>End-to-end simulations into active cable receiver | Active cable receiver electrical compliance point. Does not include DFE. Channel models of this usage model can contain fixed reference active cable receiver equalization. |



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# SDLA channel de-convolution and de-embedding

- Given a good set of channel S-Parameters, a clear model of SAS TC can be obtained for jitter and AC parametric measurements

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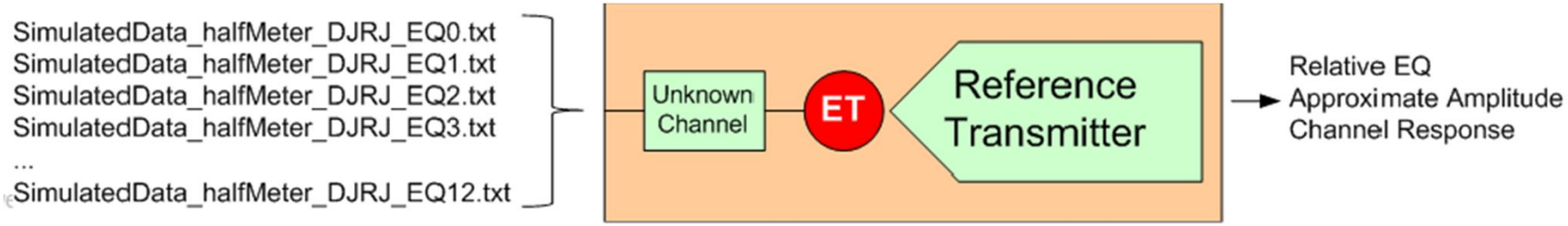
# Another.. Better way? A brief treatise on the "PMC or SAS-3 Eye" Considered as a replacement for WDP

- Method: ***PMC (11-416r2 section X, 5.7.5.7.3)***
  - Capture a frequency-rich pattern, as close as practical to TX (CT/IT, but could also be CR/IR or any non-compliant point available)
  - First without emphasis
  - Next with the emphasis under test (repeat for each emphasis)
  - A very good pattern is the BCT training pattern (including Manchester codes & frame markers). PRBS-15 or 31 would do also. IDLE is not as accurate for amplitude estimation.
  - Extract pulse responses
  - For each emphasis' pulse response, extract the least-square-error TX FFE required to transform
  - the no-equalization pulse response into the current emphasis' pulse response.
  - Extract low-frequency TX amplitude (MPLA)
  - Normalize the coefficients relative to MPLA
  - Compute the variation between equalization steps (Delta C / MPLA) and compare to spec.
  - Compute the variations of MPLA per equalization step and compare to spec.
- *PMC's method requires a virtual compliance point (ET). However, it always de-embeds any channel, even the package, without having to measure any S parameters.*



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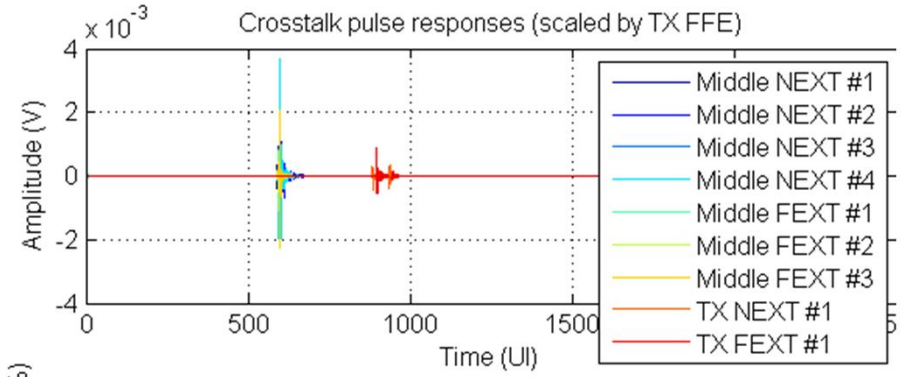
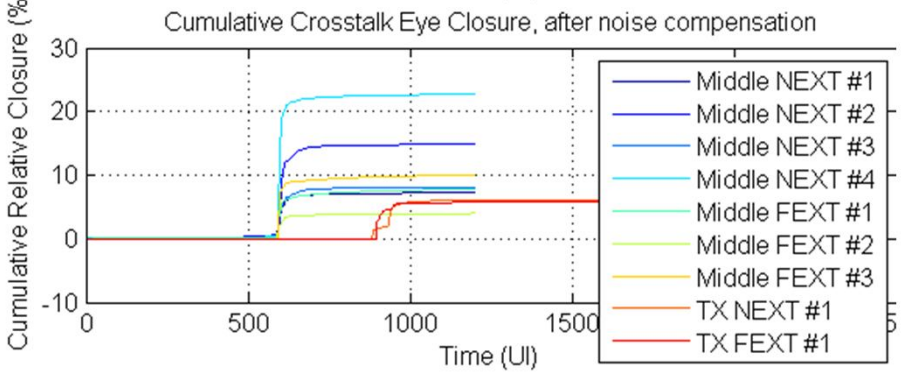
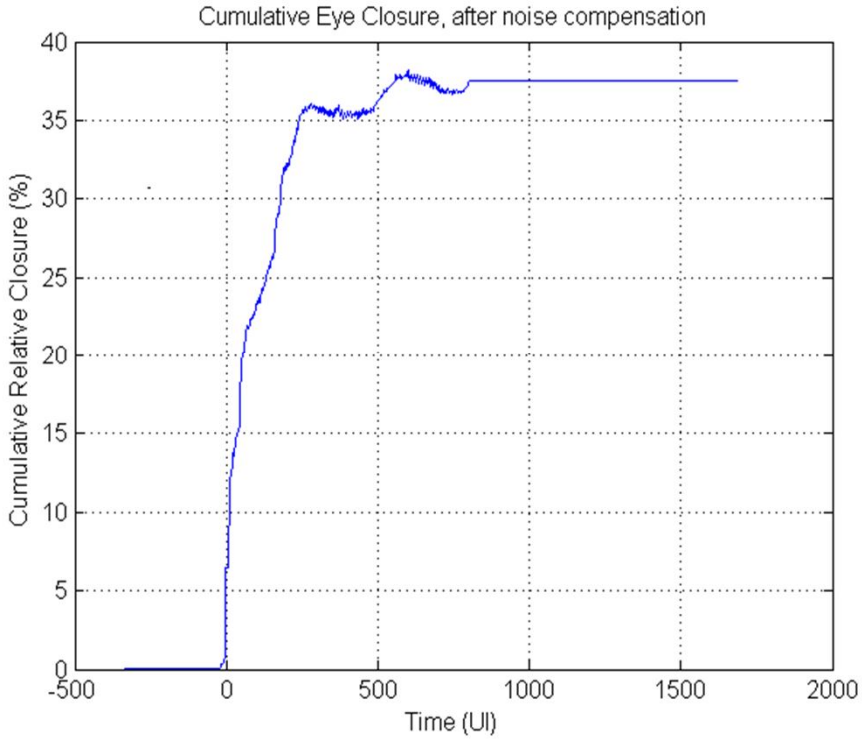
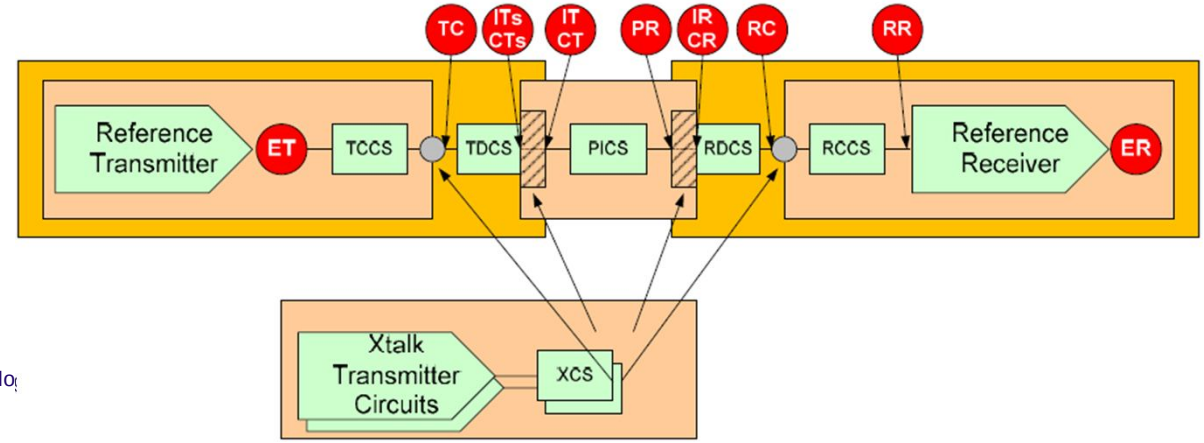
# SAS-3 brings an advanced set of crosstalk models into the channel evaluation and simulation process.



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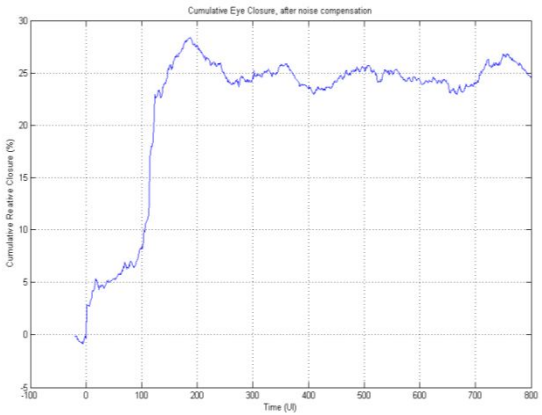
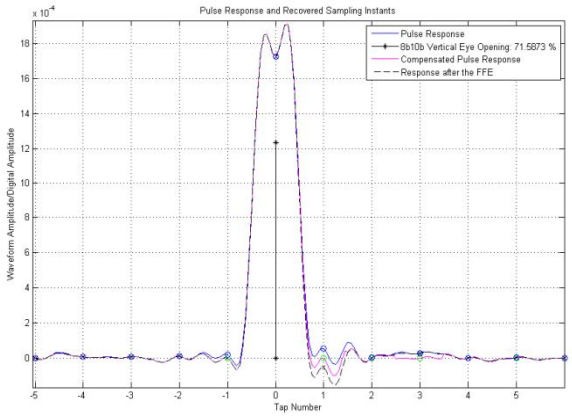
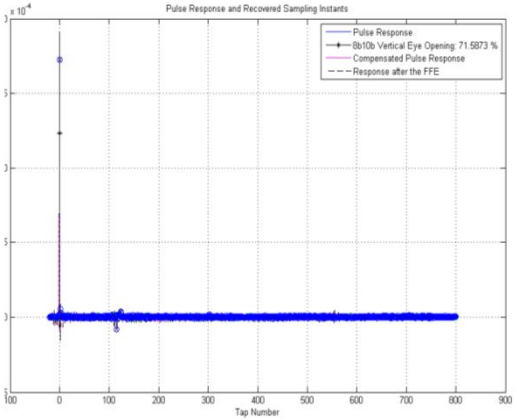
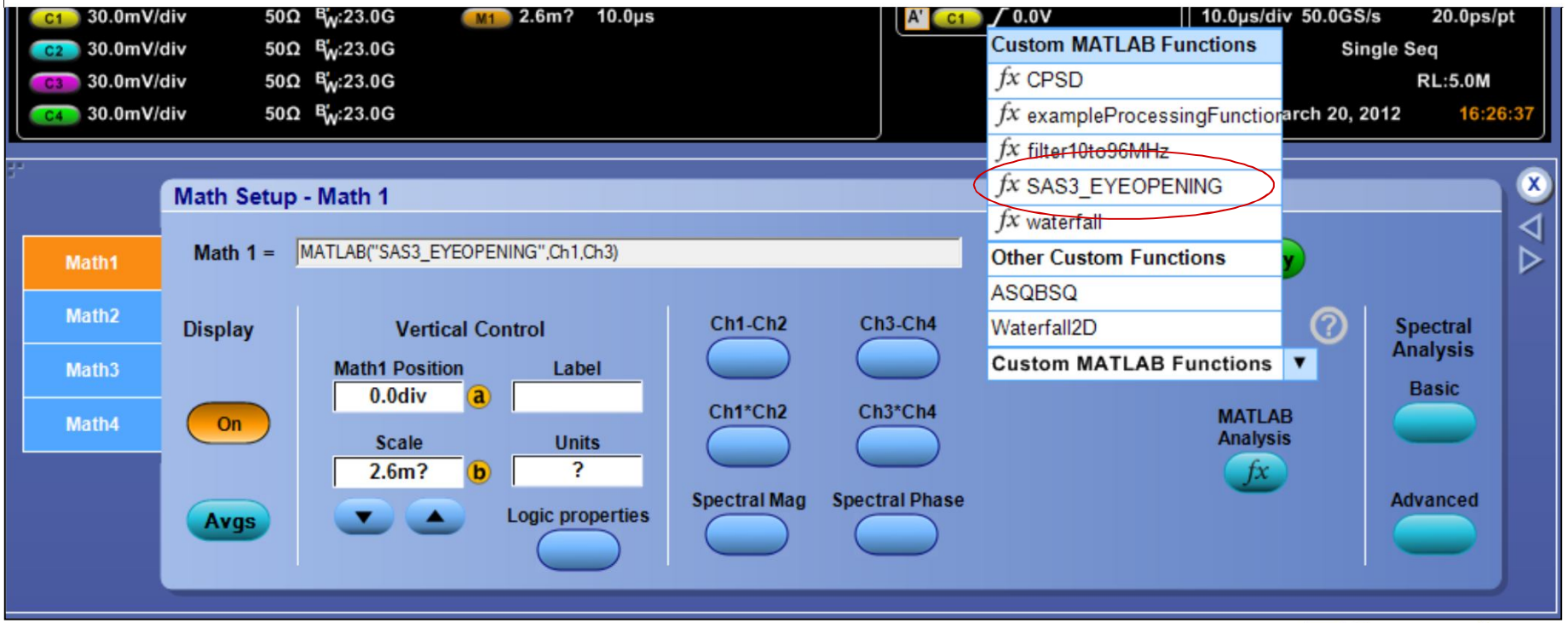
# SAS-3 Eye integrated into Scope's MATLAB services



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# Preliminary SAS-3 Tx PreC, PostC Requirements

**Table 34 — Transmitter waveform command set and transmitter circuit response**

| Description | COEFFICIENT 1[a] | COEFFICIENT 2[a] | COEFFICIENT 3[a] | Vpk(k+1)-Vpk(k) (mV) | v1(k+1)-V1(k) (mV) | v2(k+1)-V2(k) (mV) | v3(k+1)-V3(k) (mV) |
|---|---|---|---|---|---|---|---|
| Hold | hold | hold | hold | -10 to 10 | -10 to 10 | -10 to 10 | -10 to 10 |
| Increase Pre-Cursor Equalization & Hold Amplitude | dec | dec | hold | | | | |
| Decrease Pre-Cursor Equalization & Hold Amplitude | inc | inc | hold | | | | |
| Increase Post-Cursor Equalization & Hold Amplitude | hold | dec | dec | | | | |
| Decrease Post-Cursor Equalization & Hold Amplitude | hold | inc | inc | | | | |

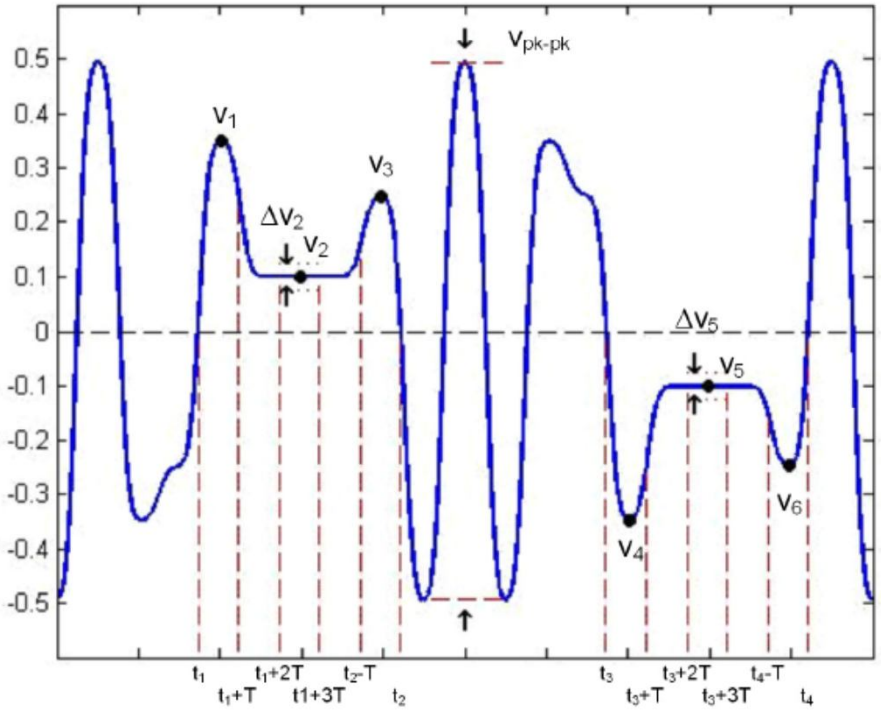


Figure 107 — 12 Gbps Reference Transmitter Circuit Output Waveform



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# SPL-2 Transmitter Training (11-036r9)
# Transmission Training Information Unit (TTIU)

- SPL-2 introduces backchannel speed negotiation and Tx runtime equalization protocol through a Manchester encoded packet tunnel in the Tx/Rx signal path.
- The SPL pattern marker is a 40 UI signal that indicates the start of the training pattern.
- The TTIU is a Manchester encoded 320 UI field that contains the 16 bit control word and 16 bit training status field.

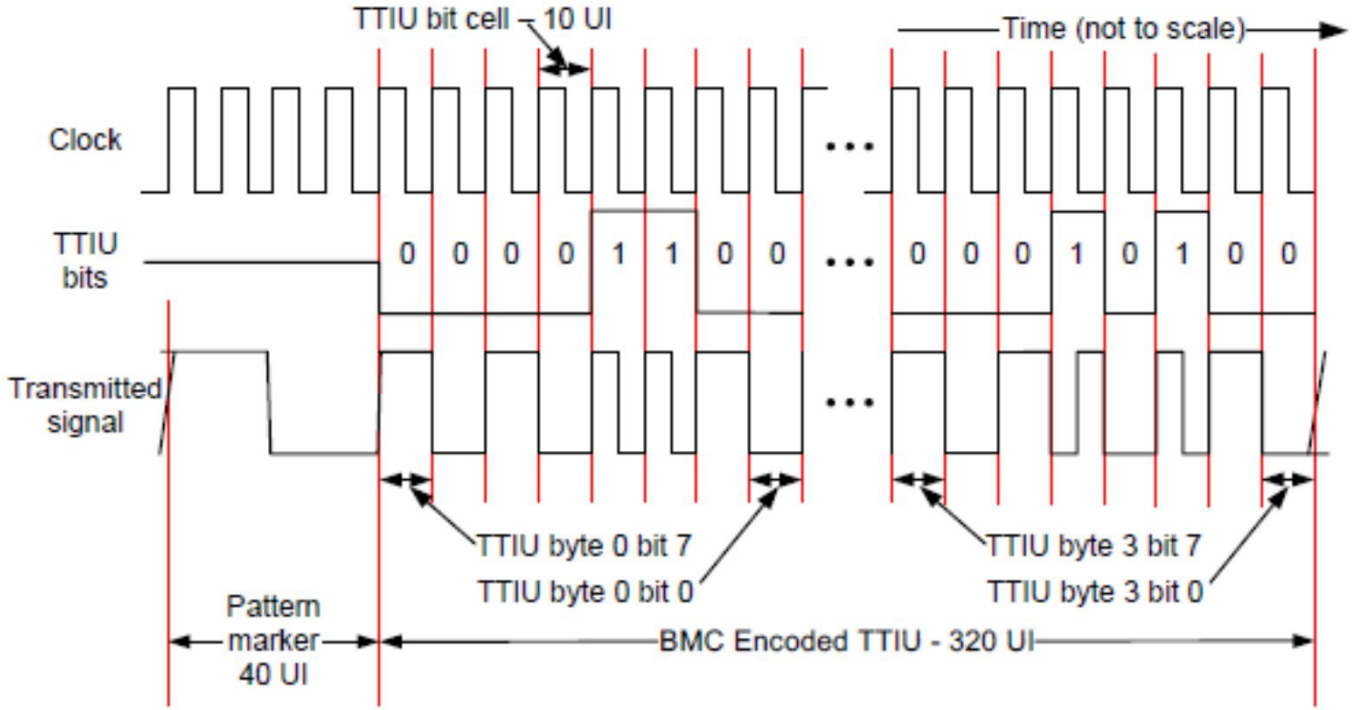
TTIU bit cell – 10 UI
Time (not to scale)
Clock
TTIU bits
0 0 0 0 1 1 0 0 ... 0 0 0 1 0 1 0 0
Transmitted signal
TTIU byte 0 bit 7
TTIU byte 0 bit 0
TTIU byte 3 bit 7
TTIU byte 3 bit 0
Pattern marker 40 UI
BMC Encoded TTIU - 320 UI

**Figure 5 — TTIU transmitter BMC encoding**



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# BUJ and relevance to multilane topologies

- Interconnect and board layout technology is advancing and the greatest area of focus is in reducing the insertion loss and Signal-to-Crosstalk ratio. Packaging parasitics cannot be ignored here either and important from both a modeling and measurement needs.
- The channel performance has to be measured as a means of identifying layout errors or inadvertent coupling which reduces the Signal-to-Crosstalk ratio (ICR). Ref[1].
- The implications of complex channel interaction as well as SERDES multiplexing method, can be observed and identified in an output signal by examining the type and amount of Bounded Uncorrelated Jitter or BUJ.
- There is a strong Cause–and-Effect relationship between Crosstalk (NEXT) and BUJ which in most systems get's classified as Random if special steps are not observed.



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# SAS-3 (r00) Specs

**5.8.4.7.1 Transmitter device signal output characteristics for trained 12 Gbps overview**

Table 41 specifies the signal output characteristics for the transmitter device for trained 12 Gbps.

**Table 41 — Transmitter device signal output characteristics for trained 12 Gbps at TC**

| Signal characteristic | Units | Minimum | Nominal | Maximum |
|---|---|---|---|---|
| Peak to peak voltage ($V_{P-P}$) [a] [b] | mV(P-P) | 850 | 1 000 | 1 200 |
| Transmitter device off voltage [c] [d] | mV(P-P) | | | 50 |
| Withstanding voltage (non-operational) | mV(P-P) | 2 000 | | |
| Rise/fall time [e] | ps | 20.8 | | |
| Reference differential impedance [f] | ohm | | 100 | |
| Reference common mode impedance [f] | ohm | | 25 | |
| Pre-cursor equalization ratio $R_{pre}$ [g] | V/V | 0.88 | | 1.67 |
| Post-cursor equalization ratio $R_{post}$ [h] | V/V | 0.88 | | 2.5 |
| VMA [i] | mV | 40 | | |
| Common mode voltage limit (rms) [j] | mV | | | 30 |
| RJ [j] [k] [l] | UI | | | 0.15 [m] |
| TJ [l] [n] | UI | | | 0.25 [o] |

[a] See 5.8.4.6.6 for the $V_{P-P}$ measurement method.
[b] Maximum voltage compliance point is at RC.
[c] The transmitter device off voltage is the maximum A.C. voltage measured at compliance points IT and CT when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).
[d] This is not applicable when optical mode is enabled.
[e] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 01b or 10b pattern (e.g., D10.2 or D21.5) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) on the physical link.
[f] See 5.8.4.7.2 for transmitter device S-parameters characteristics.
[g] Ratio measured with post-cursor equalization disabled. When both pre-cursor and post-cursor equalization are active the maximum observed $R_{pre}$ may be as high as 3.8 at the VMA limit.
[h] Ratio measured with pre-cursor equalization disabled, When both pre-cursor and post-cursor equalization are active the maximum observed $R_{post}$ may be as high as 5.5 at the VMA limit.
[i] Measured as the maximum of 100 x $(v_1 + v_4) / v_1$, 100 x $(v_2 + v_5) / 2$, or 100 x $(v_3 + v_6) / 3$ when $v_2 > 100$mV (see figure 120).
[j] This is a broadband limit. For additional limits on spectral content, see figure 113 and table 37.
[k] The RJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3)(see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2) with SSC disabled. RJ is 14 times the RJ 1 sigma value, based on a BER of $10^{-12}$. For simulations based on a BER of $10^{-15}$, the RJ specified is 16 times the RJ 1 sigma value.
[l] The measurement shall include the effects of the JTF (see 5.8.3.2).
[m] 0.15 UI is 12.5 ps at 12 Gbps.
[n] The TJ measurement shall be performed with a repeating 0011b or 1100b pattern (e.g., D24.3) (see the phy test patterns in the Protocol-Specific diagnostic page in SPL-2). If the transmitter device supports SSC, then this test shall be performed with both SSC enabled and SSC disabled. TJ is equivalent to BUJ + RJ. ISI is minimized by the test pattern.
[o] 0.25 UI is 20.8 ps at 12 Gbps.

- The Jitter and AC parametric measurements currently in the draft SAS-12G spec section are simple operations which can be performed within the DPOJET framework today.
- Particular attention needs to be paid to Jitter. Notice it's no longer performed on a Scrambled-0 or JTPAT. Rather it's done on a double bit timed clock (1100) pattern.
- The dual and potential four channel aspect of SAS requires jitter tools which are BUJ aware.
- Key SAS silicon players have been working with Tek for the last two years on advancing the state of our BUJ tools which are currently state of the art today.
- Notice there is no WDP for SAS at 12G. It's been proposed that it be replaced with SAS-3 Eye.



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# Preliminary SAS-3 JTF Requirements Reference T10/11-221r4 R0

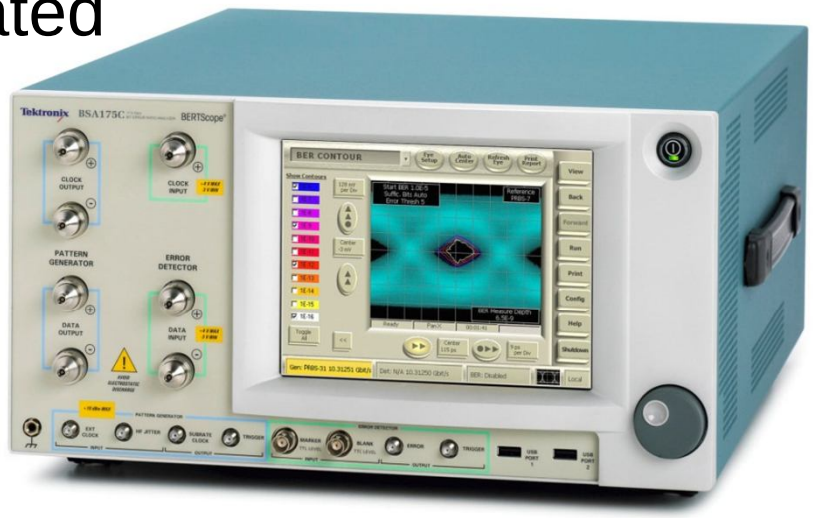
**Table 28 — JTF parameters**

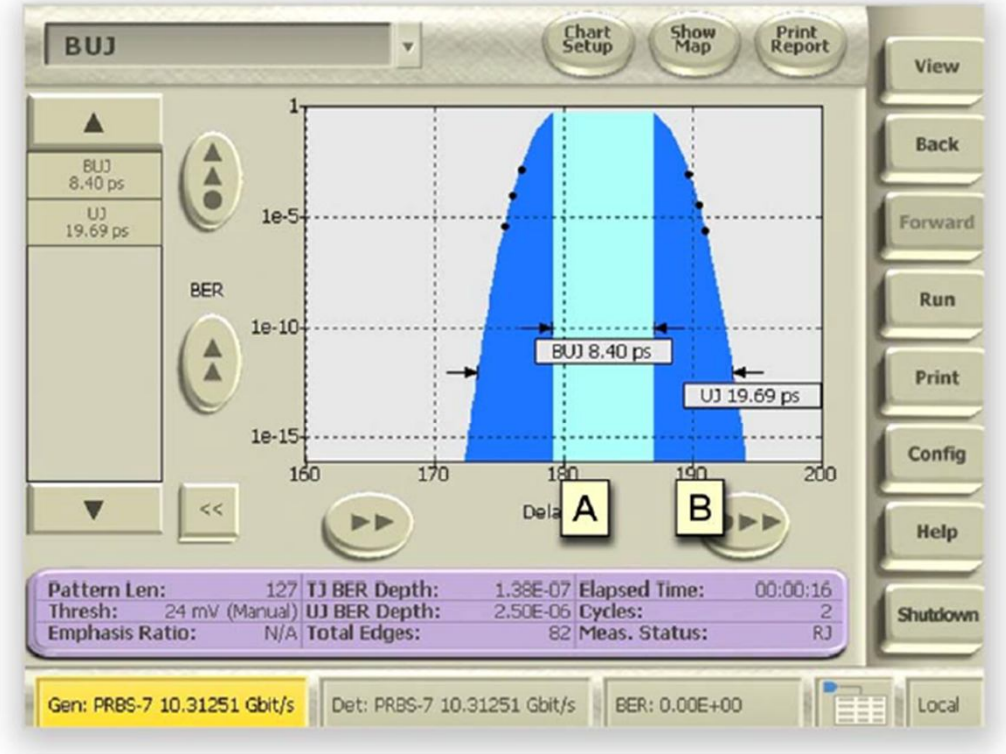
| Characteristic | Untrained | | Trained without SSC support | | | | Trained with SSC support | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1.5 Gbps | 3 Gbps | 1.5 Gbps | 3 Gbps | 6 Gbps | 12 Gbps | 1.5 Gbps | 3 Gbps | 6 Gbps | 12Gbps |
| JTF -3 dB point (kHz) [a] [b] | 900 ± 500 | 1 800 ± 500 | 900 ± 500 | 1 800 ± 500 | 3 600 ± 500 | 3 600 ± 500 | 1 300 ± 500 | 1 838 ± 500 | 2 600 ± 500 | ~~3~~2 600 ± 500 |
| JTF slope (dB/decade) | 20 | 20 | 20 | 20 | 20 | 20 | 40 | 40 | 40 | ~~2~~40 |
| Attenuation at 30 kHz ± 1 % (dB) [c] | N/A | N/A | N/A | N/A | N/A | N/A | 61.5 ± 1.5 | 67.5 ± 1.5 | 73.5 ± 1.5 | ~~N/A~~73.5 ± 1.5 |
| Maximum Peaking (dB) | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 |

[a] For untrained or trained without SSC support this value equals $f_{baud}/1\,667 \pm 500$ kHz.
[b] For trained with SSC support this value equals $(f_{baud})^{0.5} \times 33.566 \times Hz^{0.5} \pm 500$ kHz.
[c] For trained with SSC support this value equals $73.5 \text{ dB} + [20 \times \log(f_{baud} / 6 \times 10^9 \text{ Hz})]$ dB ± 1.5 dB.
[d] For the above equations, $f_{baud}$ is expressed in Hz (i.e., 1.5 GHz for 1.5 Gbps, 3.0 GHz for 3 Gbps, 6.0 GHz for 6 Gbps).

# BERTScope Bounded Uncorrelated Jitter ***Measurements***

- Classification of Rj and BUJ requires deep analysis into the lower probability regions of the cumulative PDF of isolated bits.
- At higher probabilities, the Truncated Gaussian nature of BUJ and Rj are in-distinguishable.



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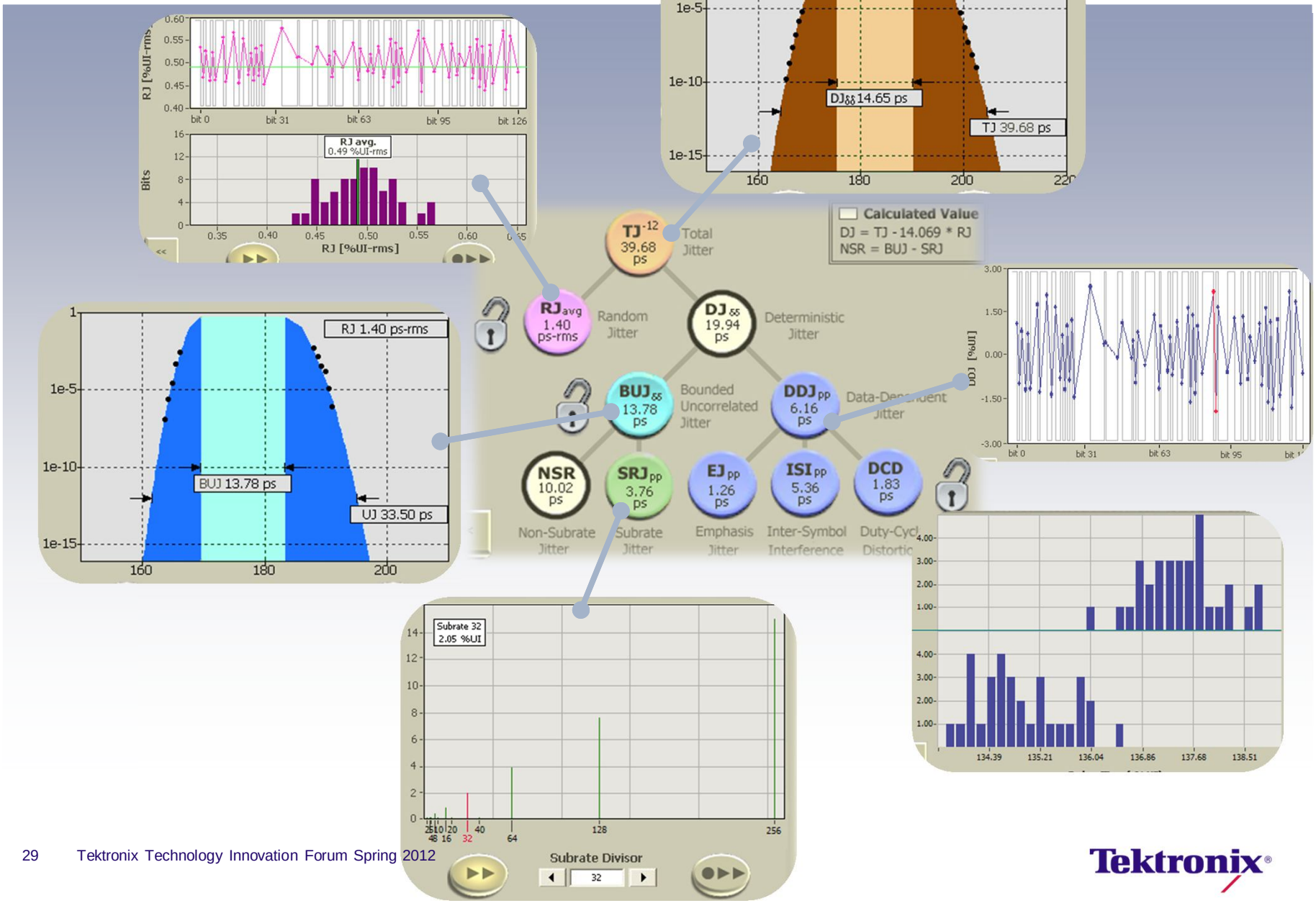
# Comprehensive Jitter Mapping tools



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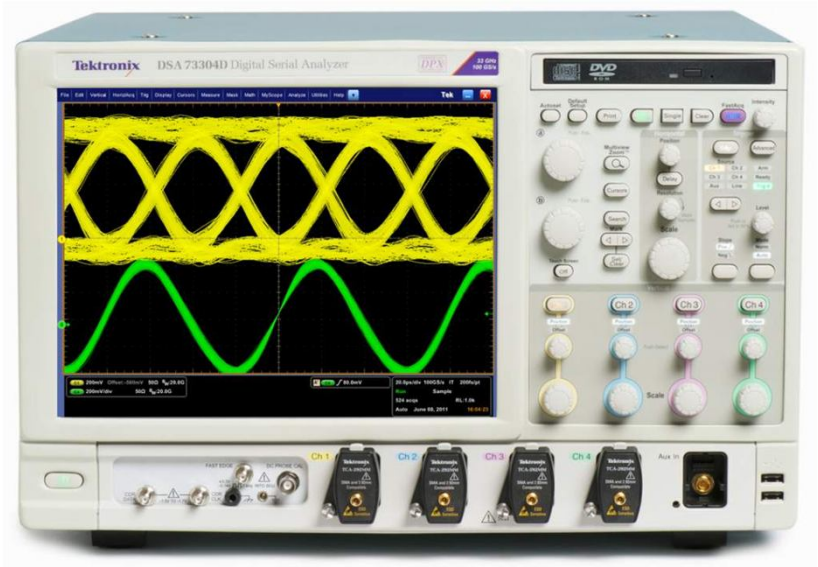
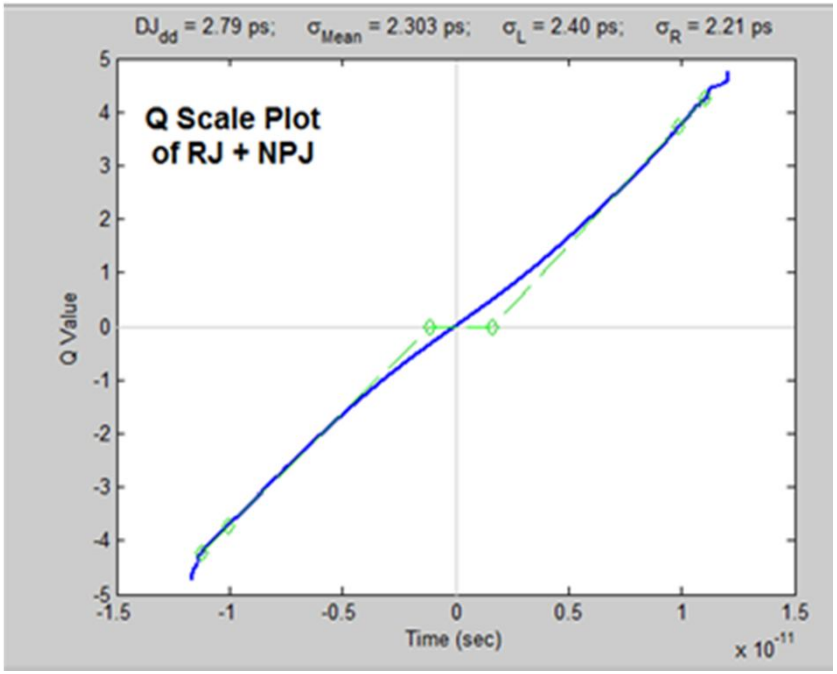
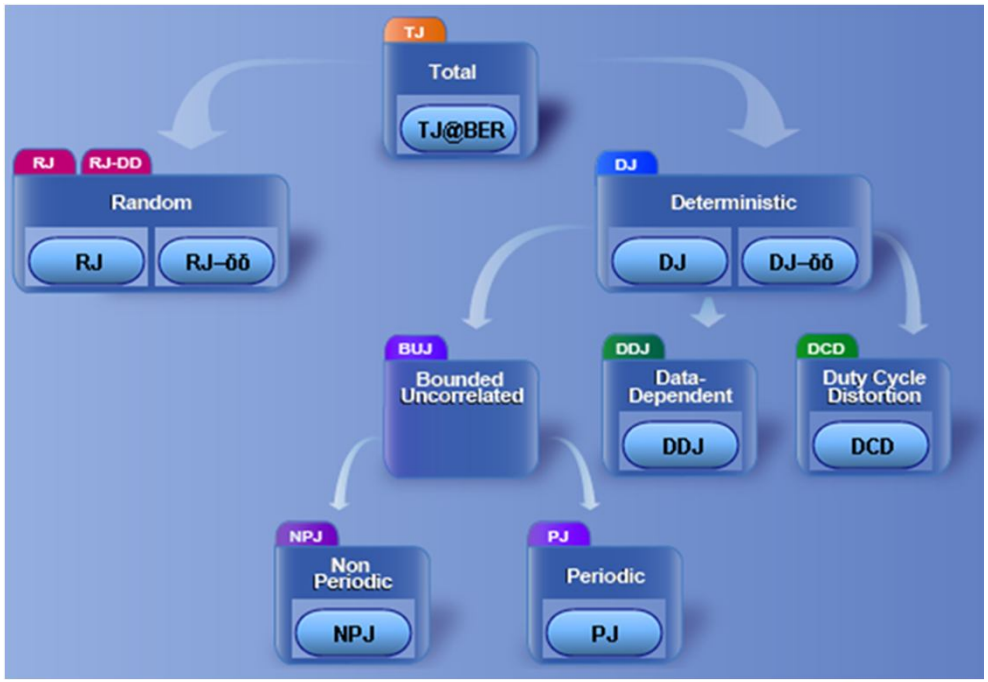
# RealTime Scope Bounded Uncorrelated Jitter ***Analysis***

- DPOJET applies straight-line fits on the Q scale of the combined Rj and NPJ CDF.
- The extent to which these left and right asymptotes are not co-linear represents the magnitude of NPJ present in the combined distribution.



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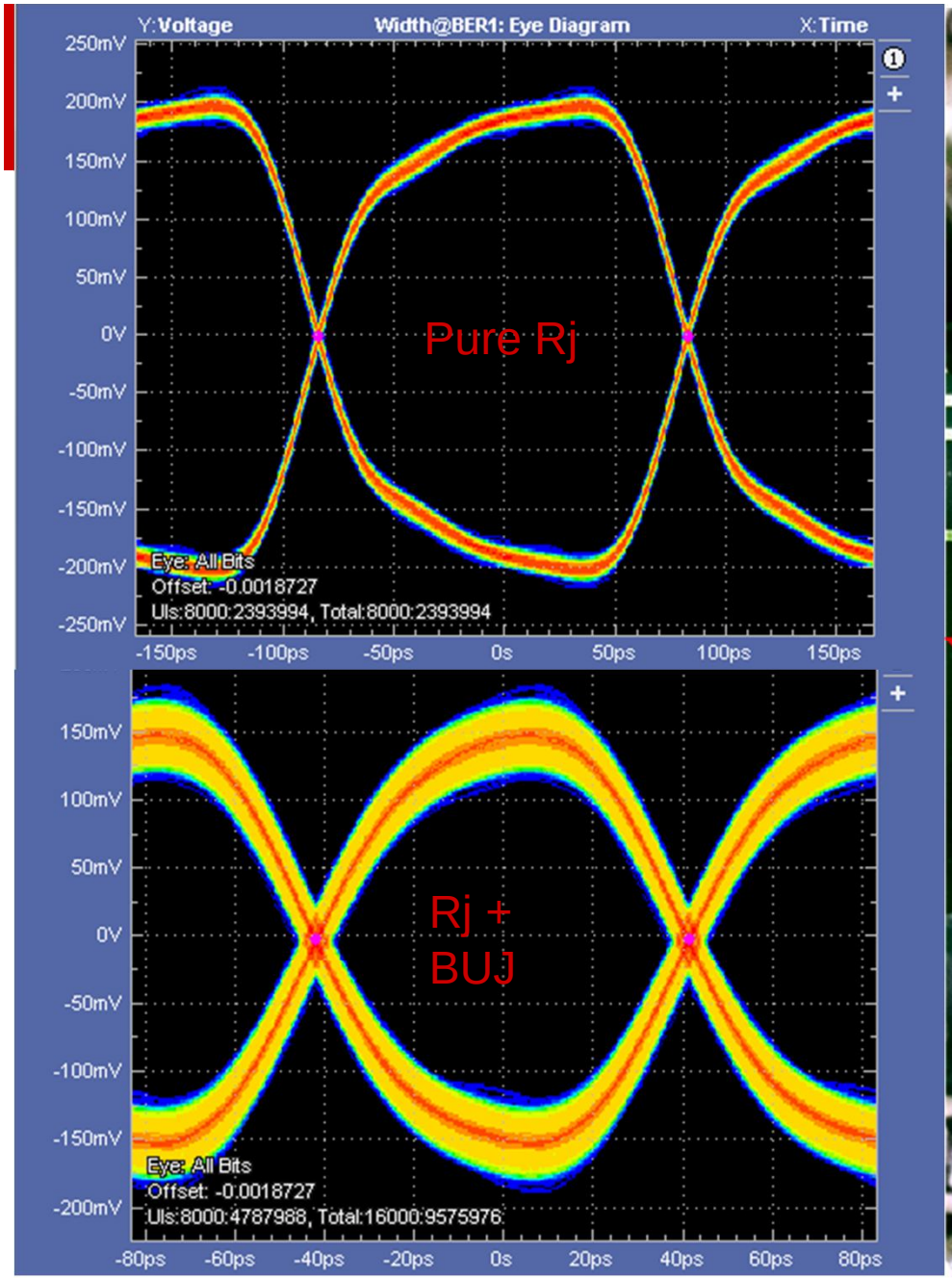
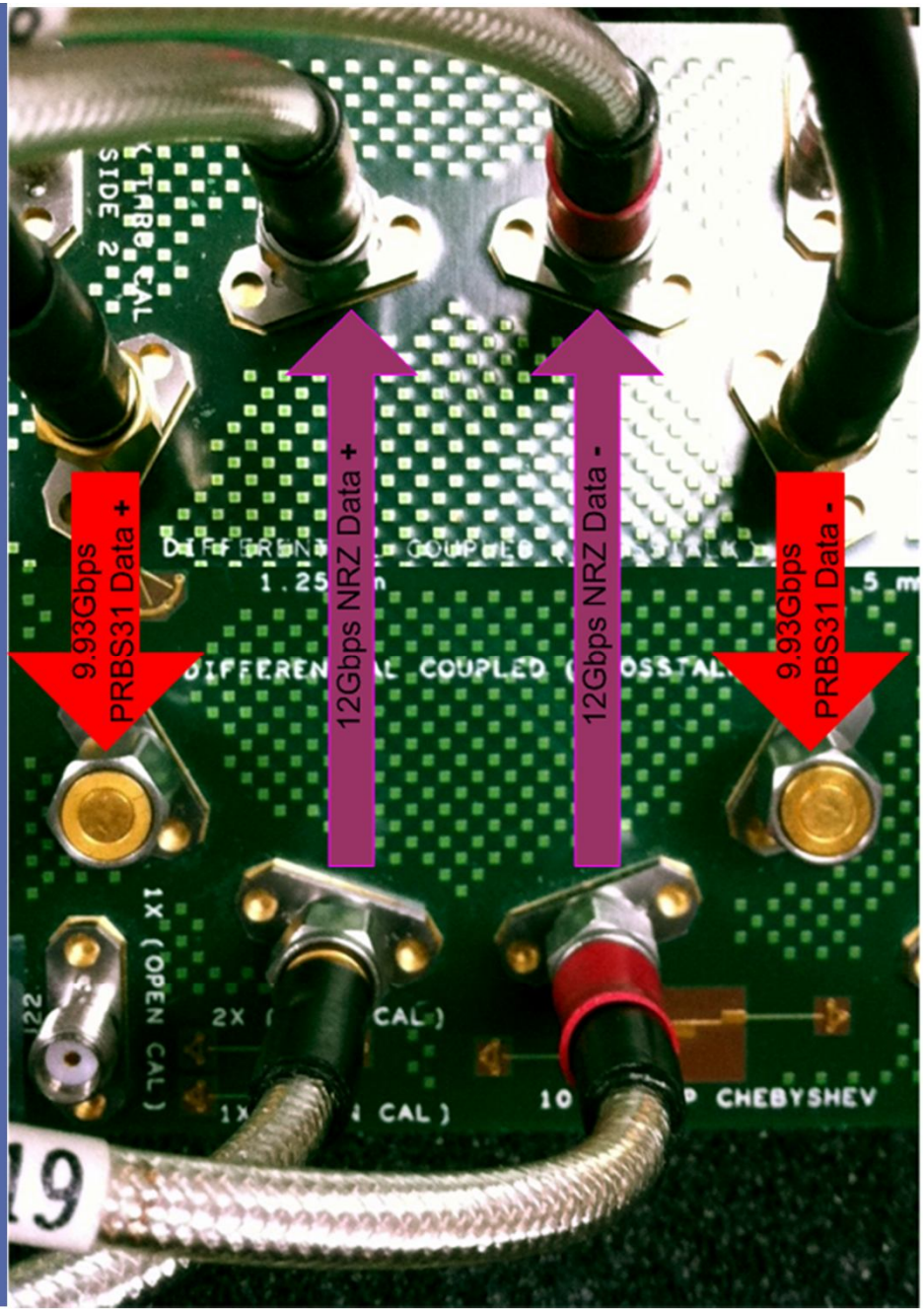

Y:Voltage
Width@BER1: Eye Diagram
X:Time
250mV
200mV
150mV
100mV
50mV
0V
-50mV
-100mV
-150mV
-200mV
-250mV
Pure Rj
Eye: All Bits
Offset: -0.0018727
Uls:8000:2393994, Total:8000:2393994
-150ps
-100ps
-50ps
0s
50ps
100ps
150ps
150mV
100mV
50mV
0V
-50mV
-100mV
-150mV
-200mV
Rj +
BUJ
Eye: All Bits
Offset: -0.0018727
Uls:8000:4787988, Total:16000:9575976
-80ps
-60ps
-40ps
-20ps
0s
20ps
40ps
60ps
80ps


9.93Gbps PRBS31 Data +
12Gbps NRZ Data +
12Gbps NRZ Data -
9.93Gbps PRBS31 Data -



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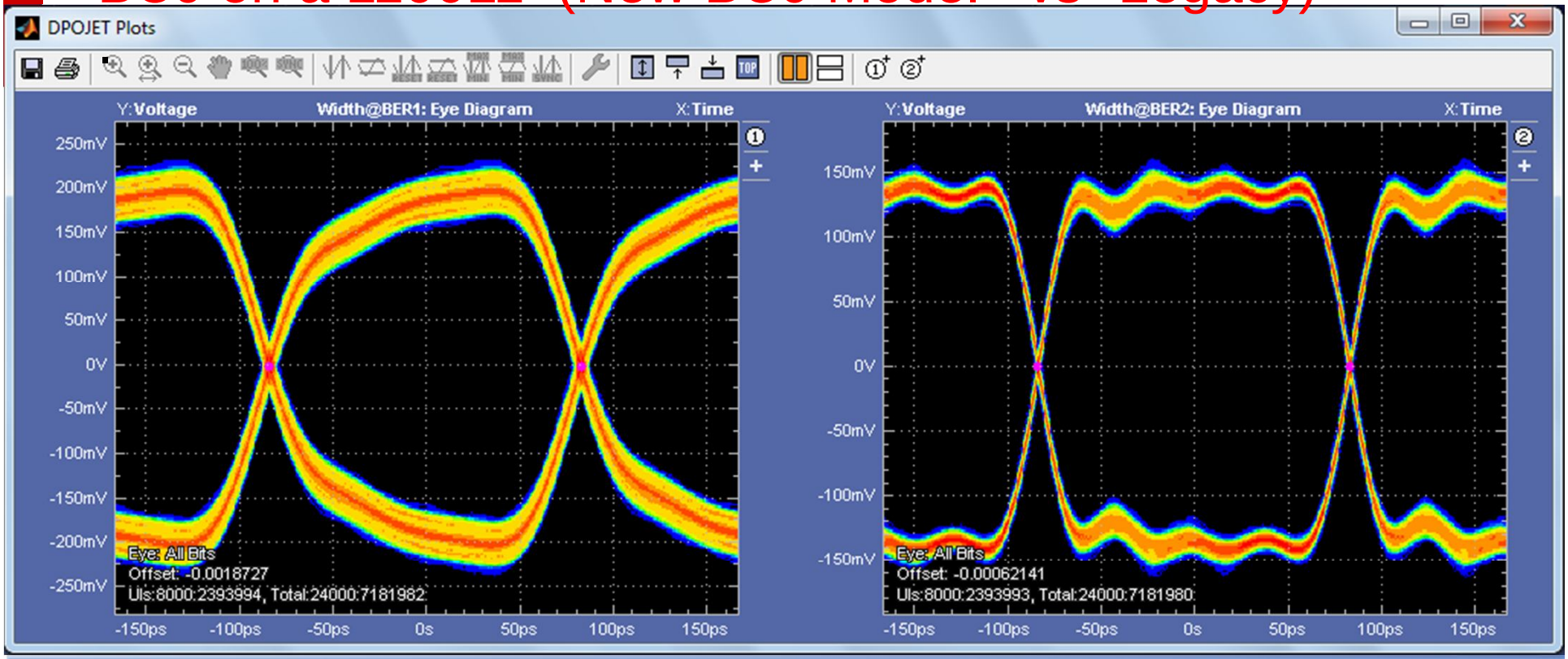
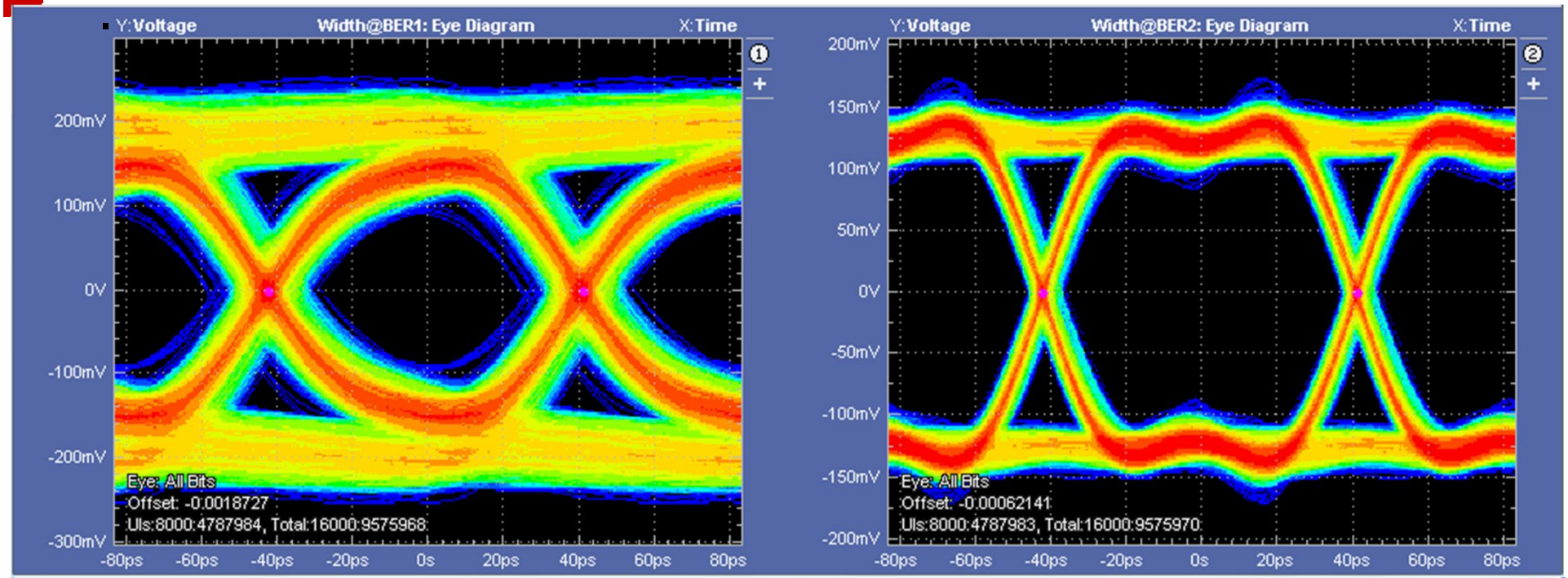
# BUJ on a 110011 (New BUJ Model –vs- Legacy)




| Description | Mean | Std Dev | Max |
|---|---|---|---|
| TJ@BER1, SAS-L1 | 14.517ps | 0.0000s | 14.517ps |
| RJ1, SAS-L1 | 666.69fs | 0.0000s | 666.69fs |
| DJ1, SAS-L1 | 2.4729ps | 40.053fs | 2.4989ps |
| TJ@BER2, SAS-L2 | 6.6669ps | 0.0000s | 6.6669ps |
| RJ2, SAS-L2 | 354.04fs | 0.0000s | 354.04fs |
| DJ2, SAS-L2 | 2.3248ps | 35.570fs | 2.3509ps |
| Width@BER1, SAS-... | 151.89ps | 19.111fs | 151.90ps |
| Width@BER2, SAS-... | 159.83ps | 25.200fs | 159.86ps |
| Clock NPJ1, SAS-L1 | 4.0639ps | | |
| Clock NPJ2, SAS-L2 | 0.0000s | | |

| Description | Mean | Std Dev | Min-cc |
|---|---|---|---|
| TJ@BER1, SAS-L1 | 24.997ps | 0.0000s | 0.0000s |
| RJ1, SAS-L1 | 1.7263ps | 0.0000s | 0.0000s |
| DJ1, SAS-L1 | 2.3614ps | 0.0000s | 0.0000s |
| TJ@BER2, SAS-L2 | 6.6687ps | 0.0000s | 0.0000s |
| RJ2, SAS-L2 | 353.06fs | 0.0000s | 0.0000s |
| DJ2, SAS-L2 | 2.3425ps | 0.0000s | 0.0000s |
| Width@BER1, SAS-... | 141.57ps | 0.0000s | 0.0000s |
| Width@BER2, SAS-... | 159.81ps | 0.0000s | 0.0000s |
| | 1.0486M | | |
| | 1.0486M | | |

# BUJ on a JTPAT (New BUJ Model –vs- Legacy)




| Description | Mean | Std Dev | Max |
|---|---|---|---|
| TJ@BER1, SAS-L1 | 45.881ps | 0.0000s | 45.881ps |
| RJ1, SAS-L1 | 844.12fs | 0.0000s | 844.12fs |
| DJ1, SAS-L1 | 35.915ps | 224.59fs | 36.074ps |
| TJ@BER2, SAS-L2 | 19.097ps | 0.0000s | 19.097ps |
| RJ2, SAS-L2 | 359.39fs | 0.0000s | 359.39fs |
| DJ2, SAS-L2 | 16.492ps | 25.389fs | 16.510ps |
| Width@BER1, SAS-... | 37.454ps | 0.0000s | 37.454ps |
| Clock NPJ1, SAS-L1 | 3.3984ps | | |
| Clock NPJ2, SAS-L2 | 0.0000s | | |

| Description | Mean | Std Dev | cc | Min-cc |
|---|---|---|---|---|
| TJ@BER1, SAS-L1 | 52.176ps | 0.0000s | 0s | 0.0000s |
| RJ1, SAS-L1 | 1.8198ps | 0.0000s | 0s | 0.0000s |
| DJ1, SAS-L1 | 35.683ps | 0.0000s | 0s | 0.0000s |
| TJ@BER2, SAS-L2 | 19.151ps | 0.0000s | 0s | 0.0000s |
| RJ2, SAS-L2 | 359.23fs | 0.0000s | 0s | 0.0000s |
| DJ2, SAS-L2 | 16.472ps | 0.0000s | 0s | 0.0000s |
| Width@BER1, SAS-... | 31.154ps | 0.0000s | 0s | 0.0000s |
| Width@BER2, SAS-... | 64.181ps | 0.0000s | 0s | 0.0000s |
| | | 1.4110M | | |
| | | 1.4110M | | |



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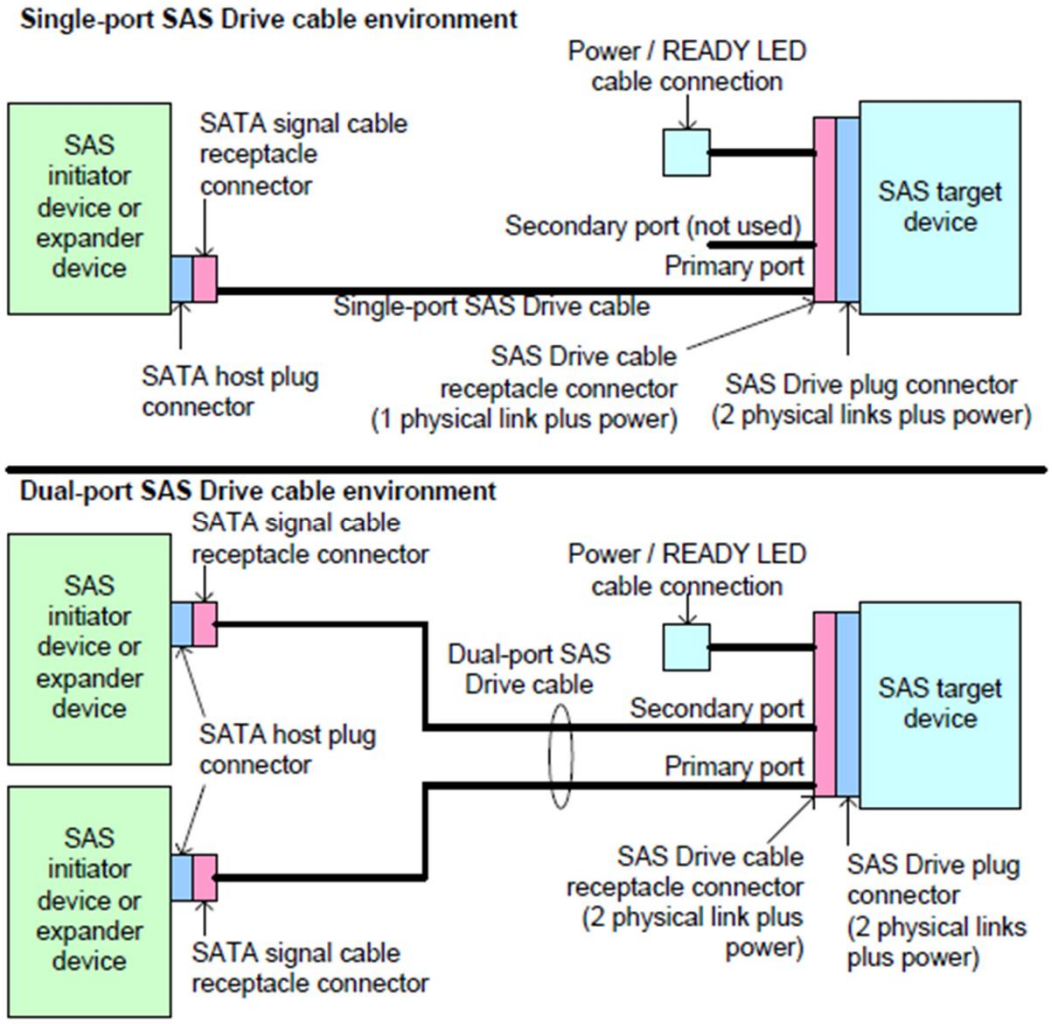
# Channel Count Considerations

## SAS comes in 1, 2, 4 and 8 channel variants.

- The Tektronix DSA7(33/25)04D Real Time Oscilloscope family offers the following interconnect specs.
- 2 Channel 100Gs/sec Sample rate at 33 GHz analog Bandwidth.
- 4 Channel 50Gs/sec Sample rate at 23.5GH analog Bandwidth.


Single-port SAS Drive cable environment
Power / READY LED cable connection
SAS initiator device or expander device
SATA signal cable receptacle connector
SAS target device
Secondary port (not used)
Primary port
Single-port SAS Drive cable
SATA host plug connector
SAS Drive cable receptacle connector (1 physical link plus power)
SAS Drive plug connector (2 physical links plus power)
Dual-port SAS Drive cable environment
SATA signal cable receptacle connector
Power / READY LED cable connection
SAS initiator device or expander device
Dual-port SAS Drive cable
Secondary port
SAS target device
SATA host plug connector
Primary port
SAS initiator device or expander device
SAS Drive cable receptacle connector (2 physical link plus power)
SAS Drive plug connector (2 physical links plus power)
SATA signal cable receptacle connector



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# SAS-3 Spec R00 BW Requirements



## 5.8 Transmitter device and receiver device electrical characteristics

### 5.8.1 General electrical characteristics

Table 30 defines the general electrical characteristics, which apply to both transmitter devices and receiver devices.

Table 30 — General electrical characteristics

| Characteristic | Units | 1.5 Gbps (i.e., G1) | 3 Gbps (i.e., G2) | 6 Gbps (i.e., G3) | 12 Gbps (i.e., G4) |
|---|---|---|---|---|---|
| Physical link rate (nominal) | MBps | 150 | 300 | 600 | 1 200 |
| Unit interval (UI) (nominal) [a] | ps | $666.\overline{6}$ | $333.\overline{3}$ | $166.\overline{6}$ | $83.\overline{3}$ |
| Baud rate ($f_{baud}$) (nominal) | Gigasymbols/s | 1.5 | 3 | 6 | 12 |
| Maximum A.C. coupling capacitor [b] | nF | 12 | | | |
| Maximum noise during OOB idle time [c] [d] | mV(P-P) | 120 | | | |

[a] $666.\overline{6}$ equals 2 000 / 3. $333.\overline{3}$ equals 1 000 / 3. $166.\overline{6}$ equals 500 / 3. $83.\overline{3}$ equals 250 / 3.

[b] The coupling capacitor value for A.C. coupled transmit and receive pairs. See 5.8.4.2 for A.C. coupling requirements for transmitter devices. See 5.8.5.2 for A.C. coupling requirements for receiver devices. The equivalent series resistance at 3 GHz should be less than 1 ohm.

[c] With a measurement bandwidth of 1.5 × $f_{baud}$ (e.g., 9 GHz for 6 Gbps), no signal level during the idle time shall exceed the specified maximum differential amplitude.

[d] This is not applicable when optical mode is enabled.



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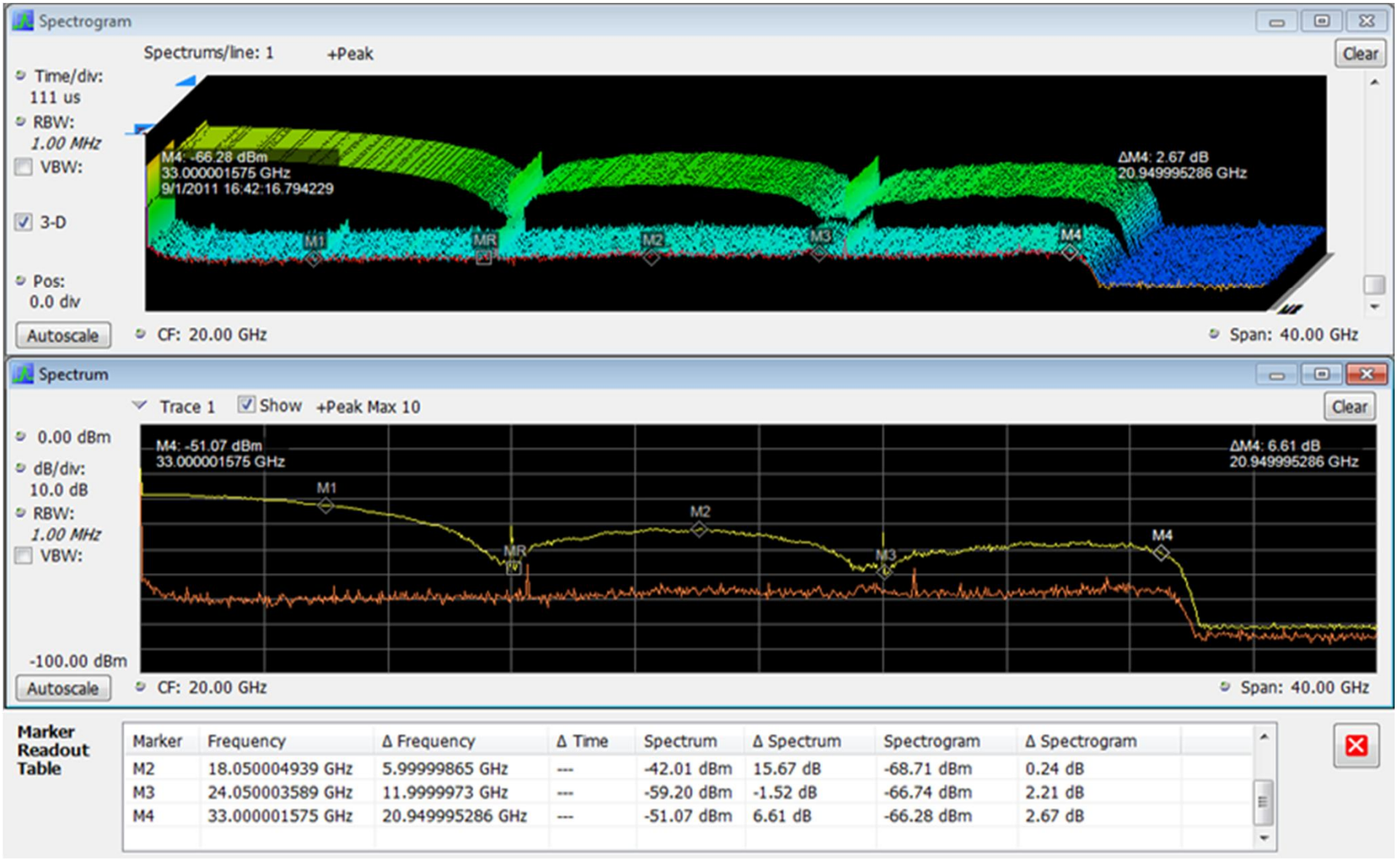
# Bandwidth Considerations
## SAS PRBS11 12G NRZ Power Spectrum

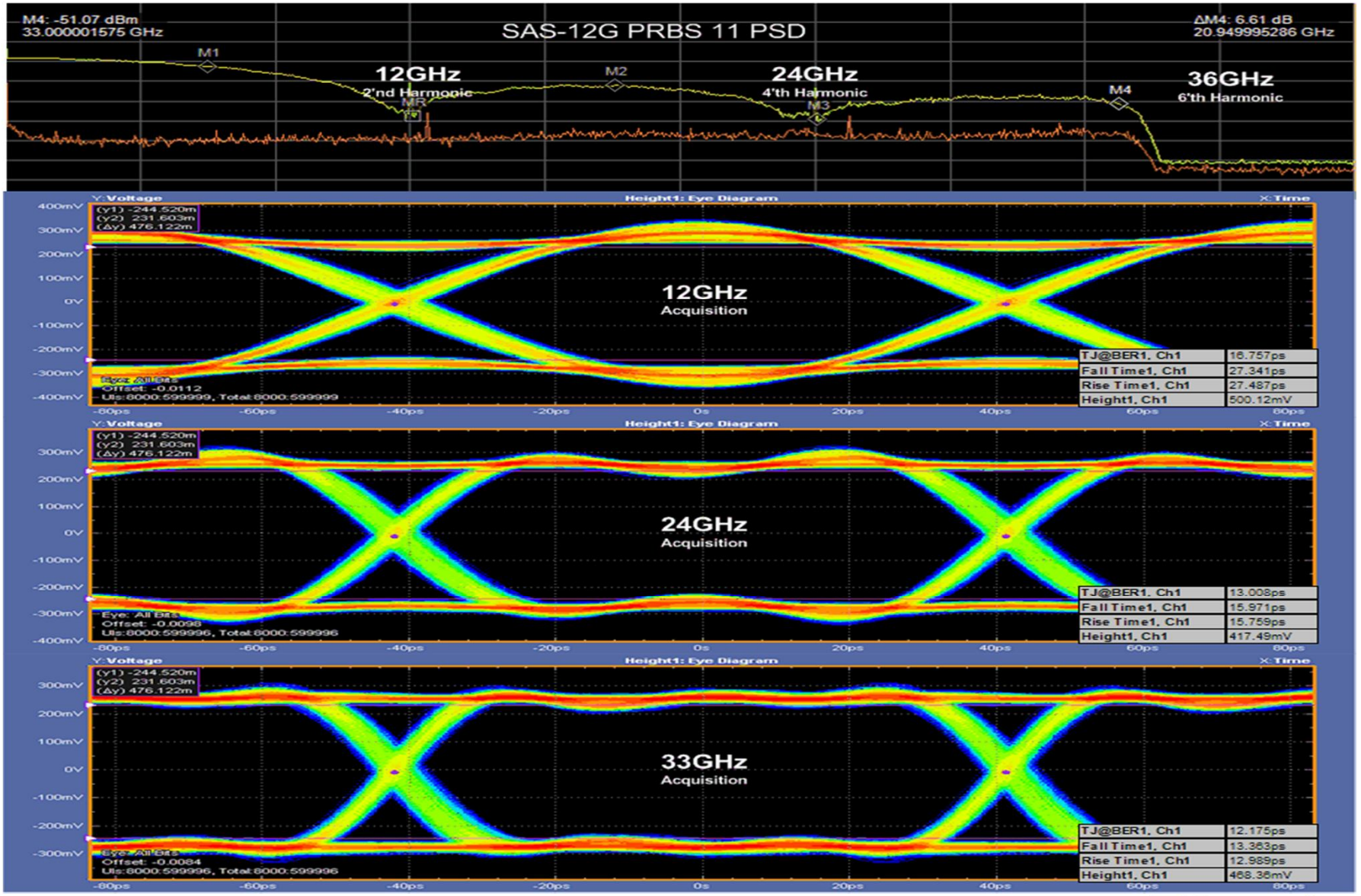



**Marker Readout Table**

| Marker | Frequency | Δ Frequency | Δ Time | Spectrum | Δ Spectrum | Spectrogram | Δ Spectrogram |
|---|---|---|---|---|---|---|---|
| M2 | 18.050004939 GHz | 5.99999865 GHz | --- | -42.01 dBm | 15.67 dB | -68.71 dBm | 0.24 dB |
| M3 | 24.050003589 GHz | 11.9999973 GHz | --- | -59.20 dBm | -1.52 dB | -66.74 dBm | 2.21 dB |
| M4 | 33.000001575 GHz | 20.949995286 GHz | --- | -51.07 dBm | 6.61 dB | -66.28 dBm | 2.67 dB |

# Bandwidth Considerations

## Signal Acquisition and bit rate harmonics



# Receiver Testing made easy

## *How the Family Fits Together*

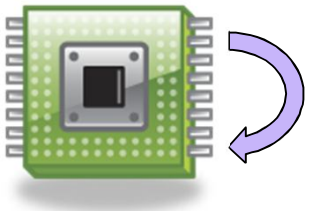
**Stressed Pattern Generator**

1

**DPP provides pre-emphasis to emulate compliant transmitter**

*From Stressed Pattern Generator*

*loopback*



*To Error Detector*

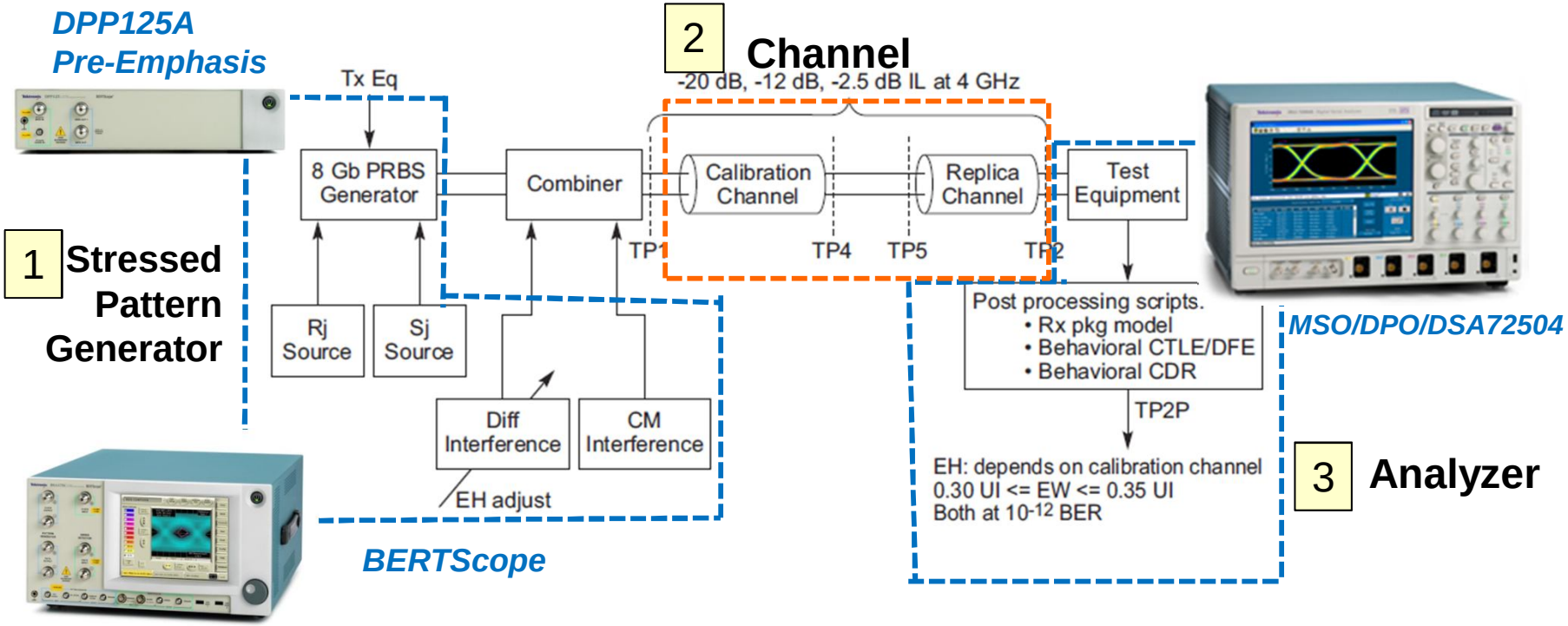
Device Under Test (DUT)

**Error Detector**

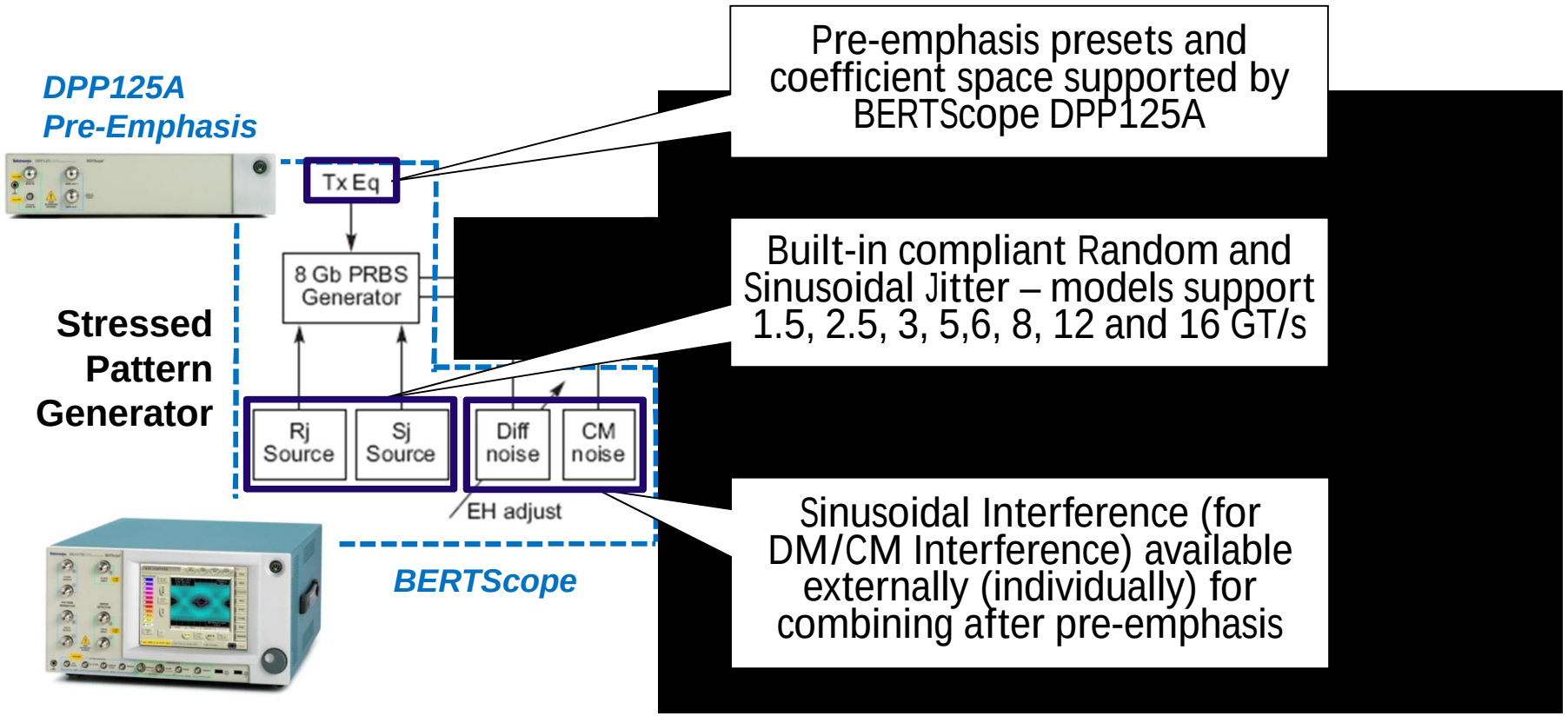
2

**CR recovers a clock from the retransmitted data from the DUT**

# Stressed Voltage Eye Calibration

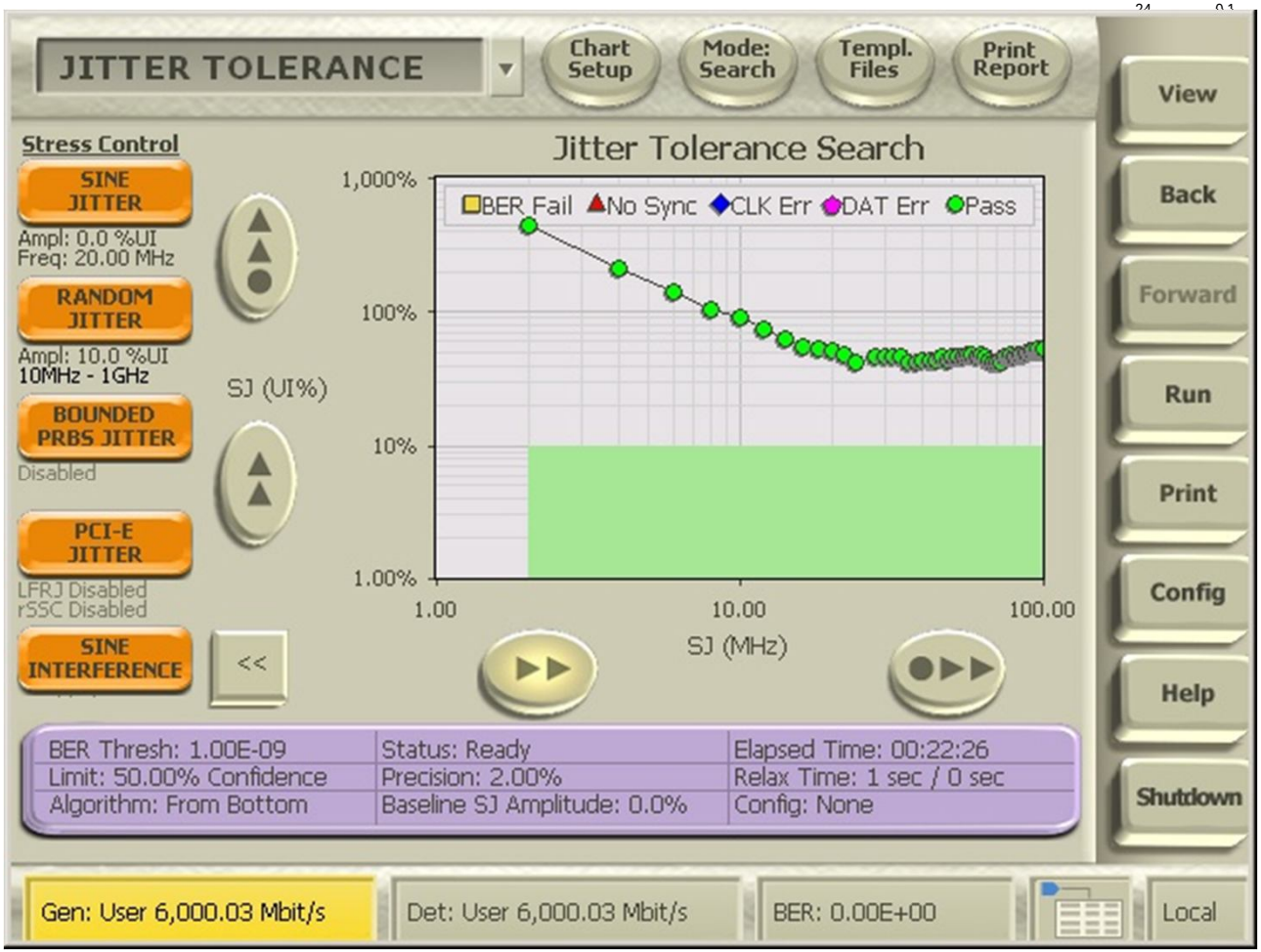


# Stressed Voltage Eye
## *Stressed Pattern Generation*


DPP125A
Pre-Emphasis
Tx Eq
8 Gb PRBS Generator
Stressed Pattern Generator
Rj Source
Sj Source
Diff noise
CM noise
EH adjust
BERTScope
Pre-emphasis presets and coefficient space supported by BERTScope DPP125A
Built-in compliant Random and Sinusoidal Jitter – models support 1.5, 2.5, 3, 5,6, 8, 12 and 16 GT/s
Sinusoidal Interference (for DM/CM Interference) available externally (individually) for combining after pre-emphasis

# Rx Results (BertScope)

- Automated Scan from 1 to 100 MHz.




| DATA T-MHz | T-SJ | SJ | Bits | Errors | BER | Status | ThreshVX | DelayPS |
|---|---|---|---|---|---|---|---|---|
| | 2 | 0.1 | 4.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| | 4 | 0.1 | 2.1 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | 6 | 0.1 | 1.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | 8 | 0.1 | 1.04 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 266.451 |
| | 10 | 0.1 | 0.9 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | 12 | 0.1 | 0.74 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | 14 | 0.1 | 0.64 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 266.451 |
| | 16 | 0.1 | 0.56 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | 18 | 0.1 | 0.54 | 6E+08 | 0 | 0.00E+00 | PASSED | 1 | 266.451 |
| | 20 | 0.1 | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | 22 | 0.1 | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 1 | 267.531 |
| | | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.44 | 6E+08 | 0 | 0.00E+00 | PASSED | -1 | 267.531 |
| | | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | -3 | 267.531 |
| | | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.42 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.46 | 6E+08 | 0 | 0.00E+00 | PASSED | -1 | 267.531 |
| | | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | | 0.48 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.5 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | -2 | 267.531 |
| | | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | -1 | 267.531 |
| | | | 0.54 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 267.531 |
| | | | 0.52 | 6E+08 | 0 | 0.00E+00 | PASSED | 0 | 266.451 |
| | | | 0.54 | 6E+08 | 0 | 0.00E+00 | LIMIT REACHED | 0 | 266.451 |



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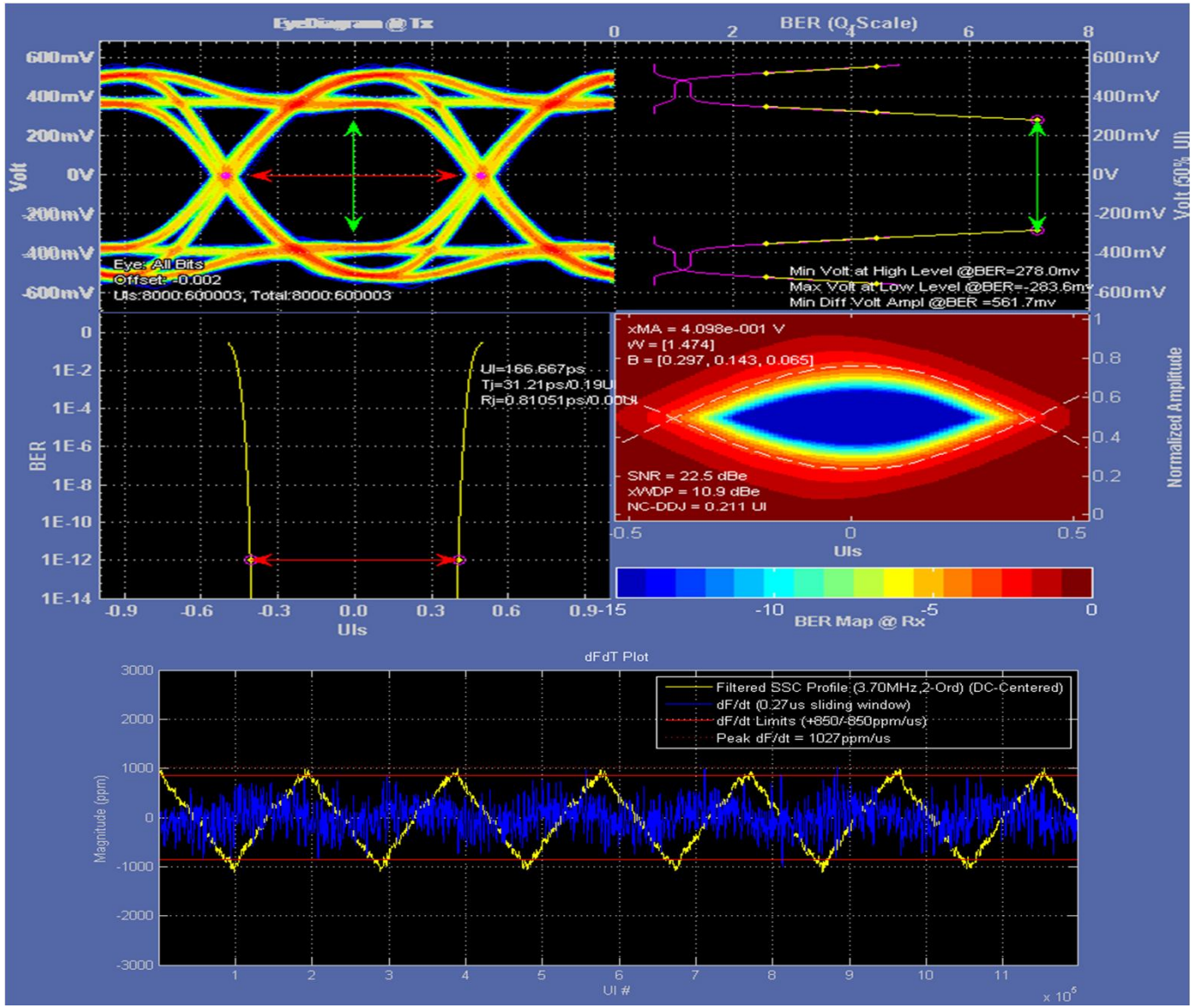
# Automated Tx Results (TekExpress full Auto)




| Test Name |
|---|
| Test 5.2.1-TX SSC Modulation Type |
| Test 5.2.2-TX SSC Modulation Frequency |
| Test 5.2.3-TX SSC Modulation Deviation and Balance |
| Test 5.2.4-TX SSC DFDT (Informative) |
| Test 5.3.1-TX Physical Link Rate Long Term Stability |
| Test 5.3.2-TX Common Mode RMS Voltage Limit |
| Test 5.3.3-TX Common Mode Spectrum |
| Test 5.3.4-TX Peak-to-Peak Voltage |
| Test 5.3.5-TX VMA and EQ |
| Test 5.3.6-TX Rise and Fall Times |
| Test 5.3.7-TX Random Jitter (RJ) |
| Test 5.3.8-TX Total Jitter (TJ) |
| Test 5.3.9-TX Waveform Distortion Penalty (WDP) |



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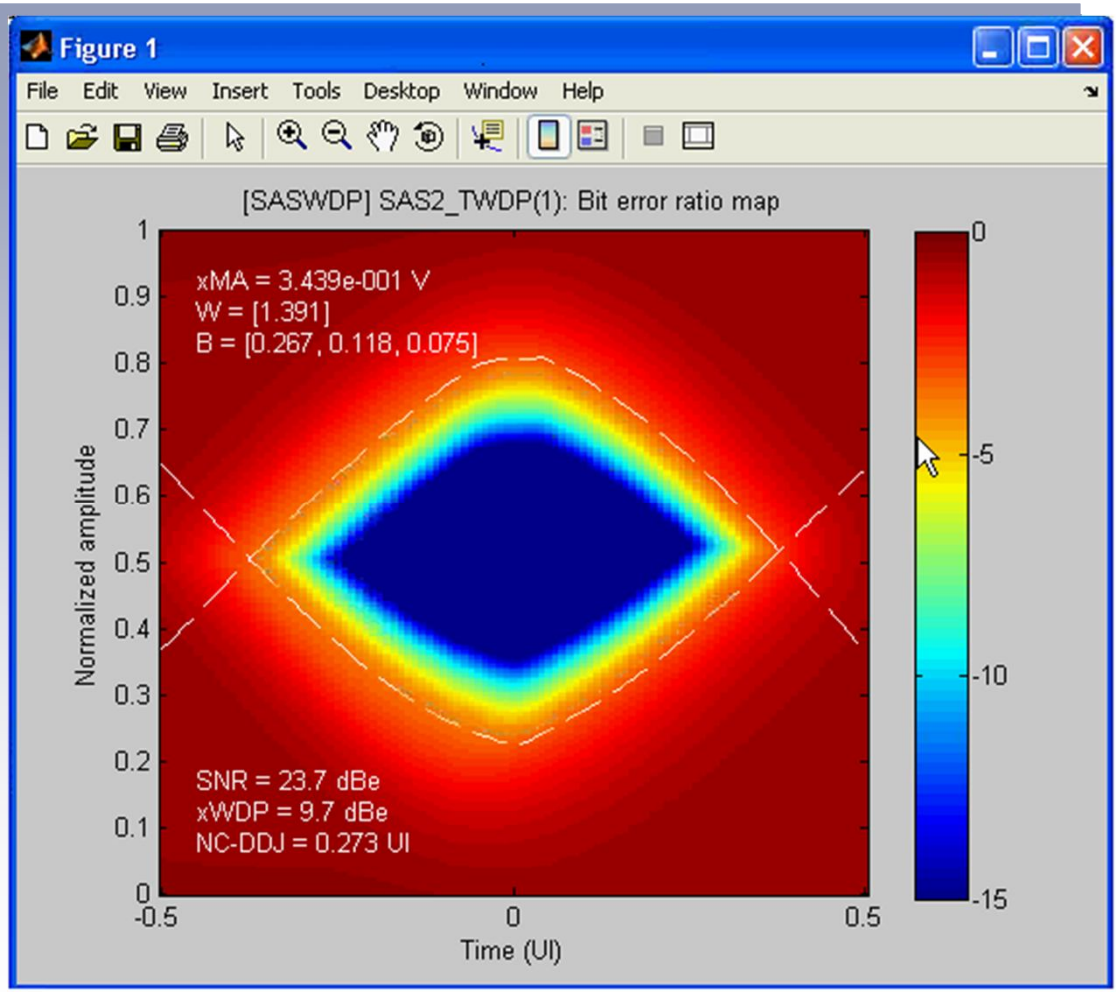
# Waveform Distortion Penalty

- Waveform Distortion Penalty (WDP/TWDP): Is a measurement method deployed in the SAS-2 spec. It uses acquired data against a simulated reference channel and DFE model, to evaluate the ratio of Non Compensable Data Dependant Jitter to it's Compensable counterpart.
- Tektronix is the *only* T&M company to negotiate licensed redistribution of WDP and TWDP as turnkey integrated measurements to our instruments.




*SAS-WDP and related methodologies contains intellectual property of Clariphy Inc.



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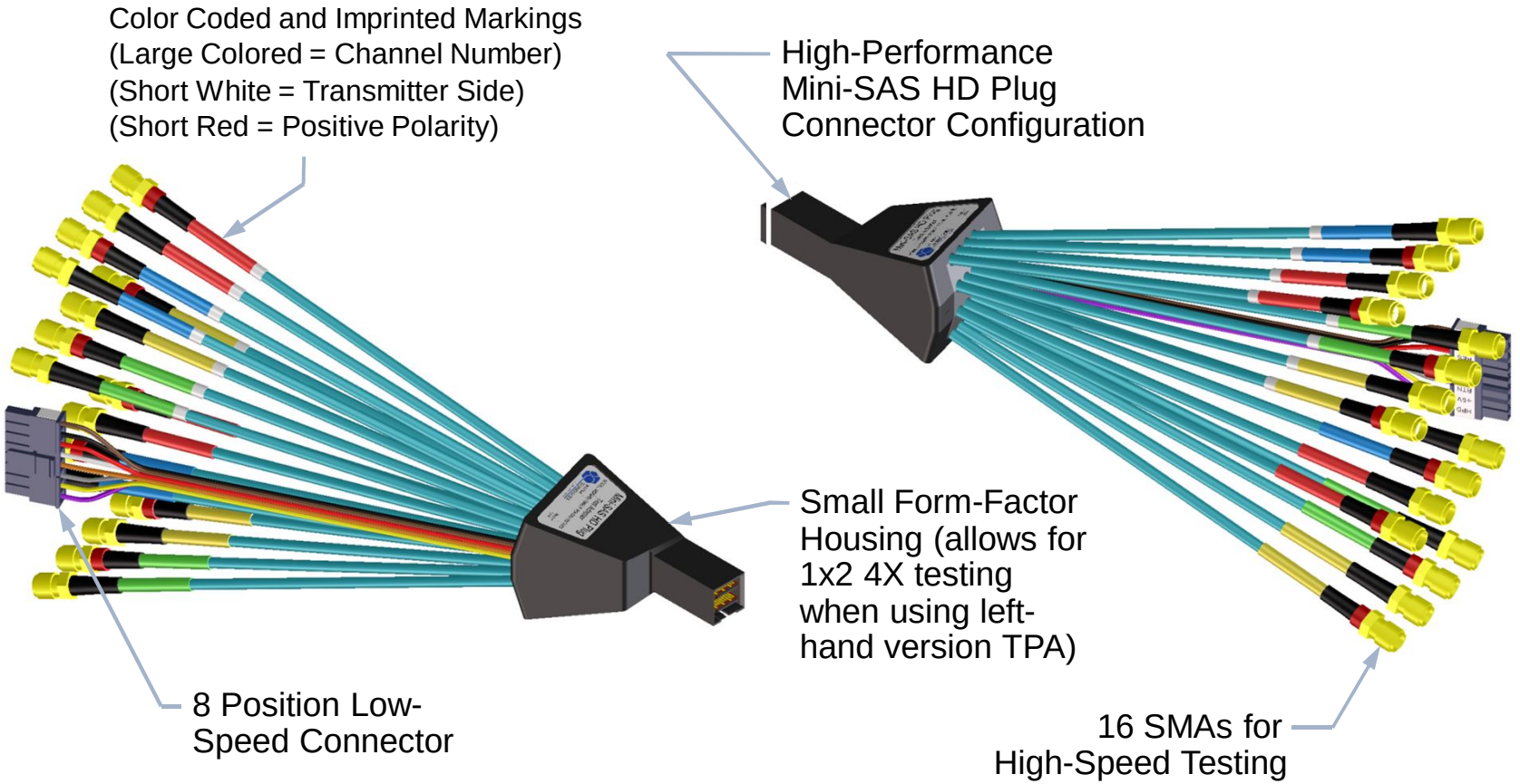
# SAS/SATA Interconnect Solutions

Tektronix and Wilder Technologies have collaborated and jointly engineered over 60 fixture and interconnect product solution configurations.

Over the last several years these solutions have become the De facto standard for all high quality device interconnect.

These products are available directly through Tektronix part numbered products or independently through Wilder at http://www.wilder-tech.com/

# Mini-SAS HD Plug Test Adapter (right-hand) Top Views



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SAS Receptacle Test Adapter
MODEL NO. SAS-TPA-R
PART NO. 600-1008-000
WILDER TECHNOLOGIES
SAS Plug Test Adapter
MODEL NO. SAS-TPA-P
PART NO. 600-1009-000
WILDER TECHNOLOGIES

# 12G SAS Instrument Solution Strategy

- Phase 0 (Silicon Designers): Transition into Phase 1 in November 2011
  - Equivalent Time Instrument: ICR, BER Contours, Far End Channel Amplitude measurements (30mV Eye), Near end Channel Transition Time measurements. All major Silicon Mfg's are using Sampling Scopes for initial evaluation of 12G SERDES'.
  - BertScope: 12G stimulus and error detector for Receiver Testing.
  - 33G Real Time Instrumentation recommended in order to perform effective Channel De-Embed of channel and fixture loss profiles. (EMC 4th harmonic proposal, presented in June 2011)
- Phase 1-2 (ODM/OEM): CY11 Q3
  - 25 GHz Real Time Instrumentation (Channel De-Embed) for Automated DFE, AC Parametric and Jitter Measurements. Manual test for now through DPOJET 12G SAS MOI.
  - 12.5G BertScope for receiver testing.
  - Support Phase 1-2 transition with test automation



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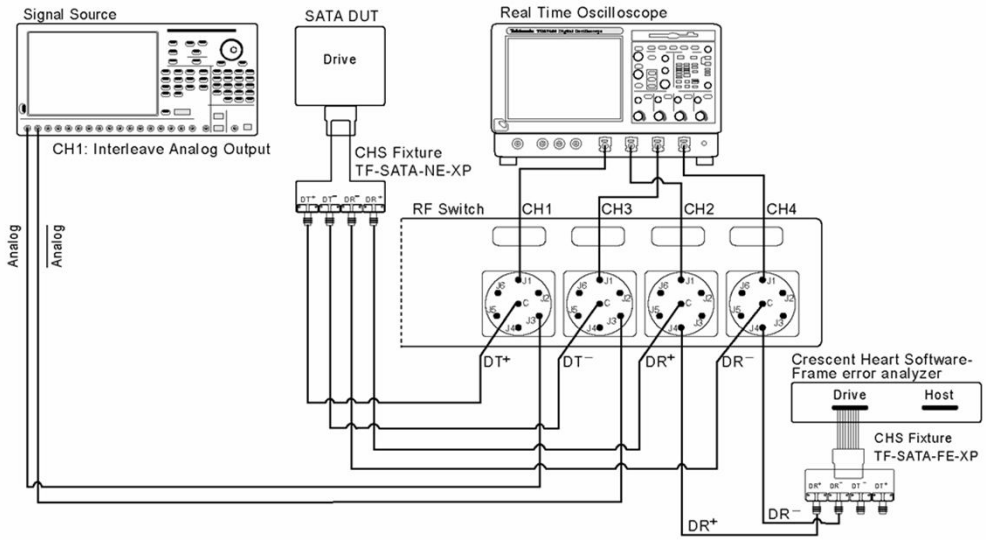
*Integrated and Automated Test Control*

# TekExpress™ Test Automation Framework




***TekExpress Instrument Topology for TSG/PHY/OOB, RSG testing***

- Simplifies Complex Measurements
- Improves Engineering Productivity
- Repeatable and Consistent results
- Automatic with no user intervention

- Complete offering includes:
  - Leading portfolio of Tektronix test instruments
    - Oscilloscopes
    - Signal generators
  - 3rd party integration with RF switch (Keithley), fixtures, API (NI), cabling, deskew, etc.
- Auto discovery of instruments using GPIB, USB, and LAN
  - 1GbE networking is used for data/waveform transport.
  - GPIB/488.2 is used for RF Switch and Power supply communications
- Test sequence automation of **all physical layer aspects of SATA and SAS**. The only solution in the industry today which can claim this.
- Full support of user defined console port scripting.
- RF-Switch automation of Keithely microwave switch matrix.
- Reporting - multiformat



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# Complete Tektronix 12G Instrument Portfolio

| | | |
|---|---|---|
| **Receiver Tests/Active Cable Tests**<br>**RSG/RMT**- Receiver Silicon and active cable characterization and compliance testing capability to 26Gbps | **BSA125C** with option **JMAP, STR** and **SF** and **DPPS125** and **CR125A** provide support for future bit-rates (12-26G) with a unique portfolio of Scope and Bert combined features. | |
| **Channel Tests**<br>**ICR**: Insertion Loss Cross Talk analysis.<br>**Rx/Tx** - Device and Host electrical channel performance, Crosstalk, Impedance and return loss | **DSA8300**<br>80E10 TDR Sampling Module for DSA8300 Sampling Scope<br>S-Parameter Analysis Software 80SICON Software for DSA8300 | |
| **Passive Cable Tests**<br>Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11. | **DSA8300**<br>80E08 TDR Sampling Module for DSA8300 Sampling Scope | |
| **PHY, TSG, and OOB Tests**<br>PHY – Signal timing stability and SSC analysis.<br>TSG – Transmitter AC parametric, Jitter, Amplitude.<br>OOB- Out Of Band signal validation | **DSA72504D**<br>DPOJET Jitter Analysis software<br>TCA-292D Coax Adapters 4 per scope | |



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# Enabling Innovation in the Digital Age